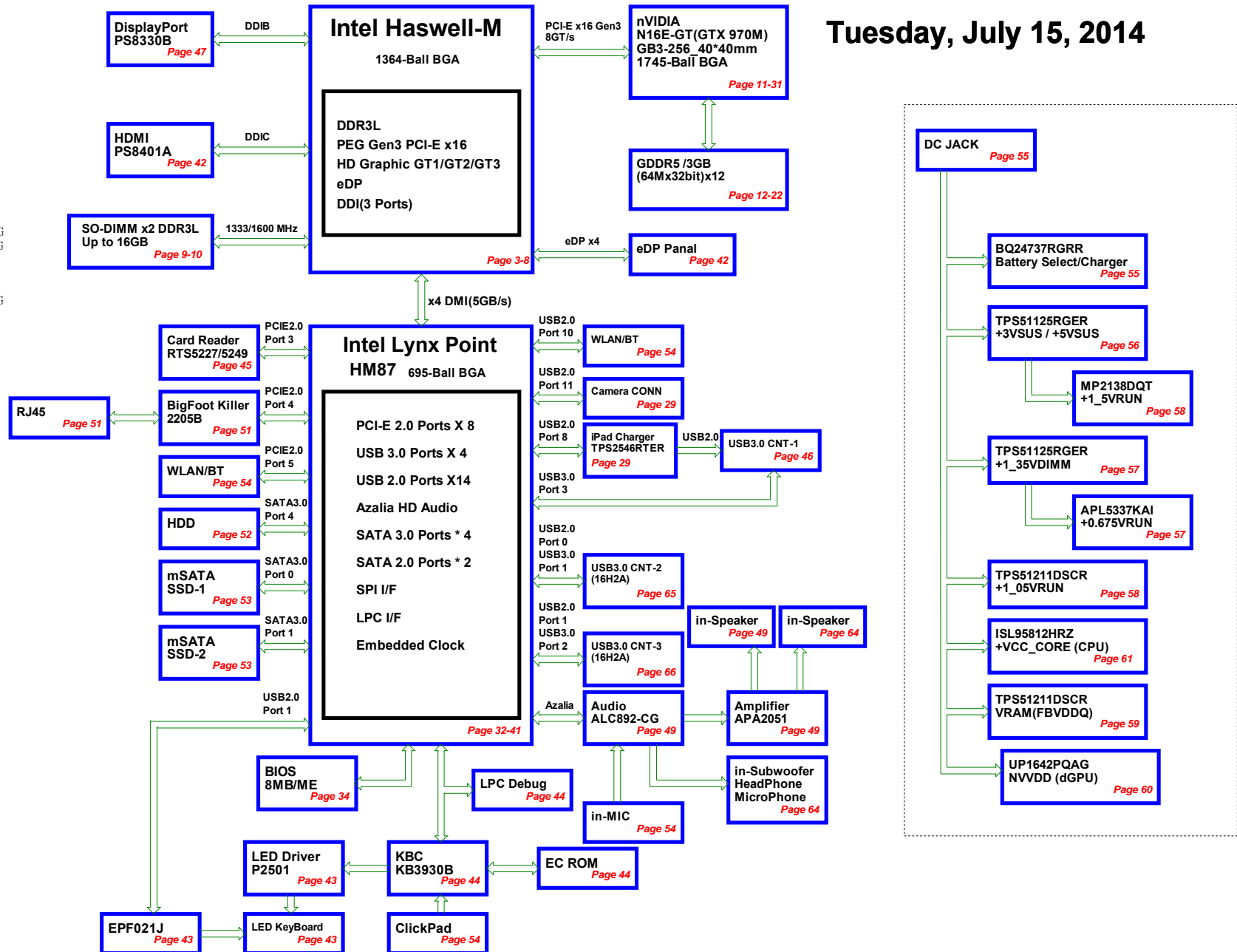
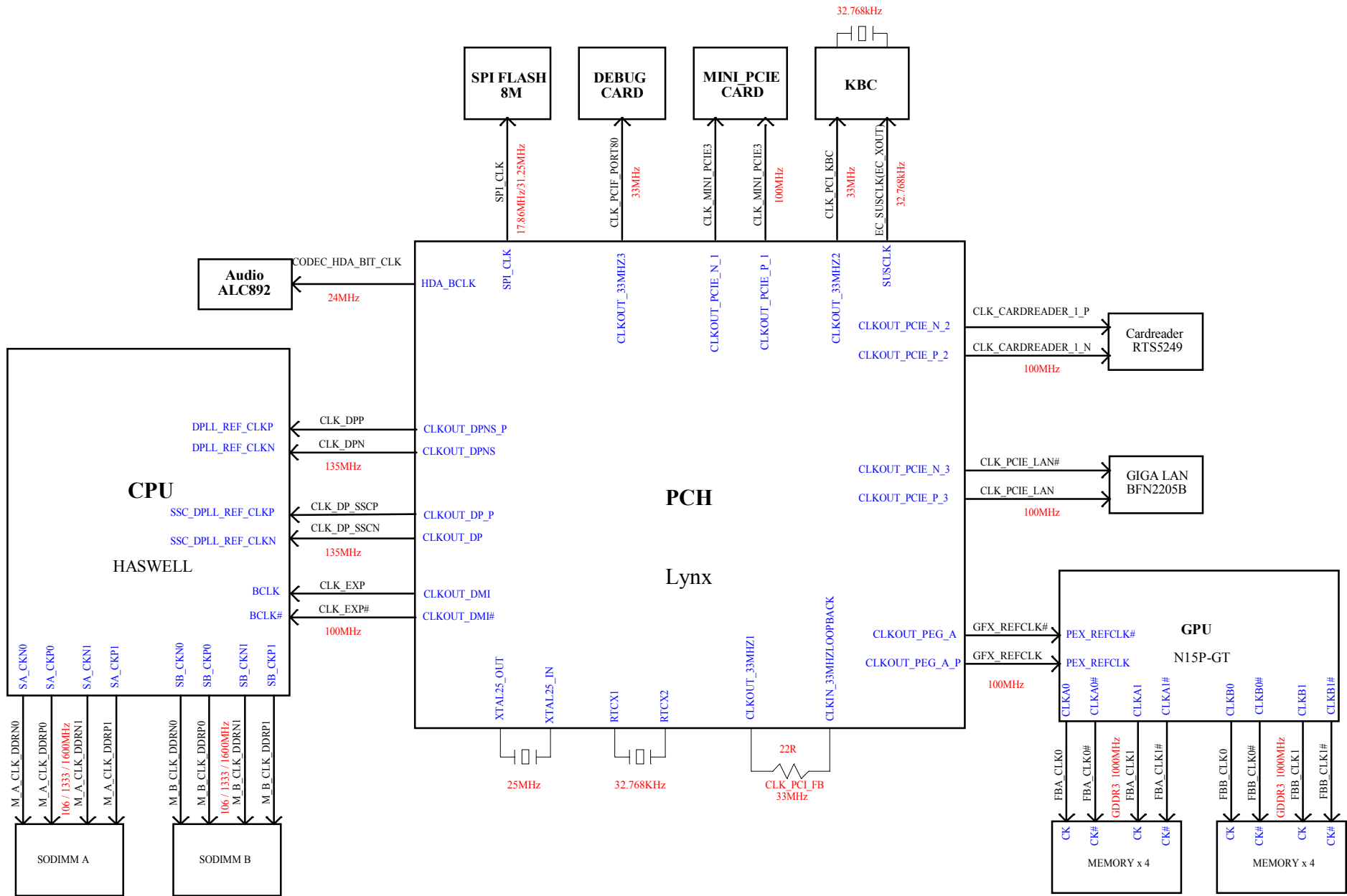


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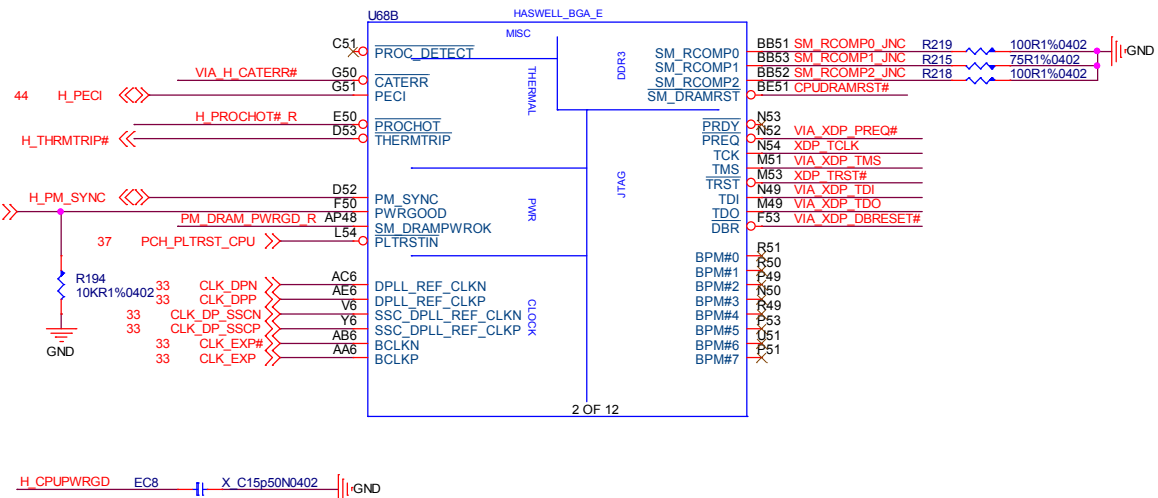
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PEG RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils
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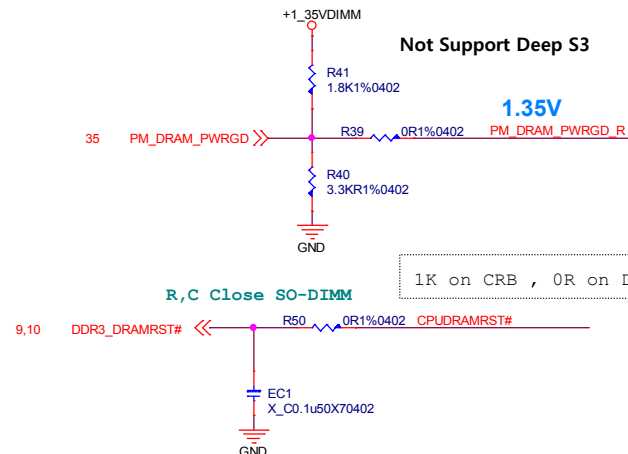
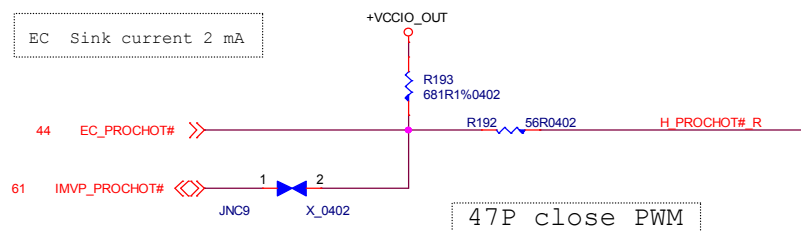


## Haswell ( CLK,MISC,JTAG )

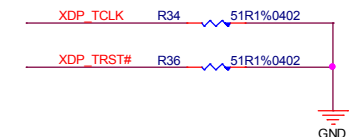
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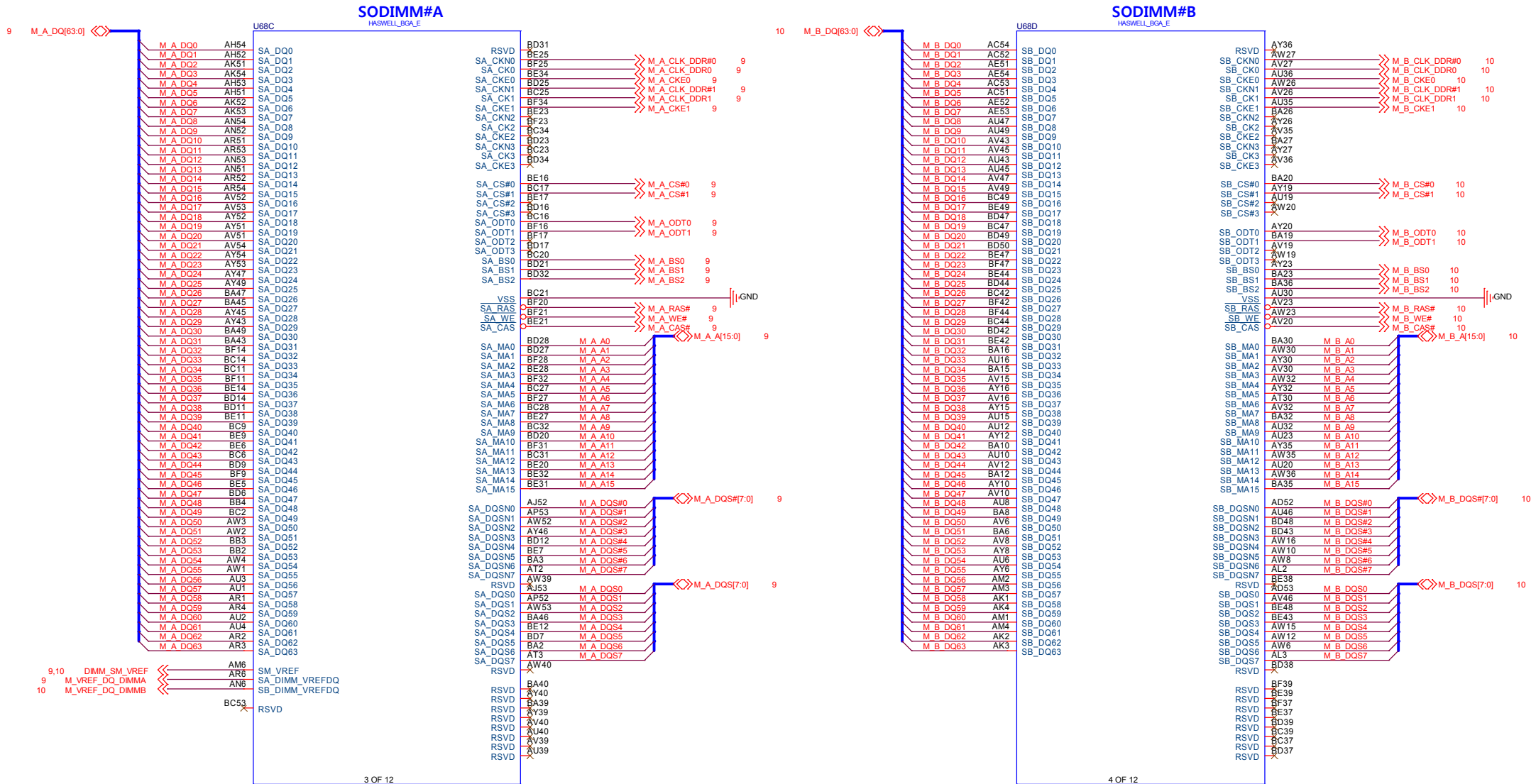
**I7 4860**



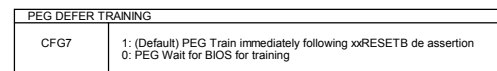
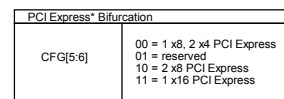
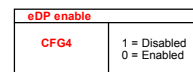
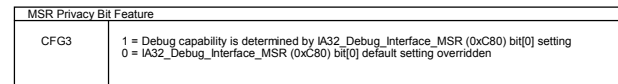
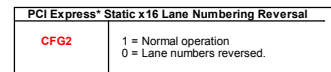
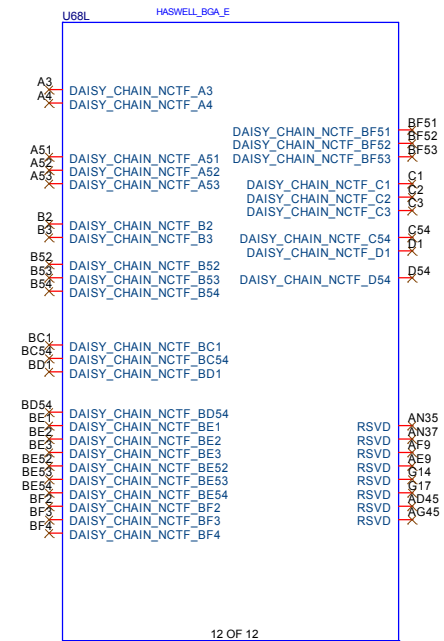
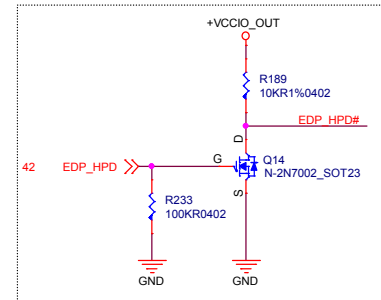
p.11 479493\_479493\_SharkBay\_HSW\_ext\_rev2.0.pdf  
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals,  
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internal bias resistances to support the removal of the  
external pull up and pull down on the board  
when debug is no longer needed.



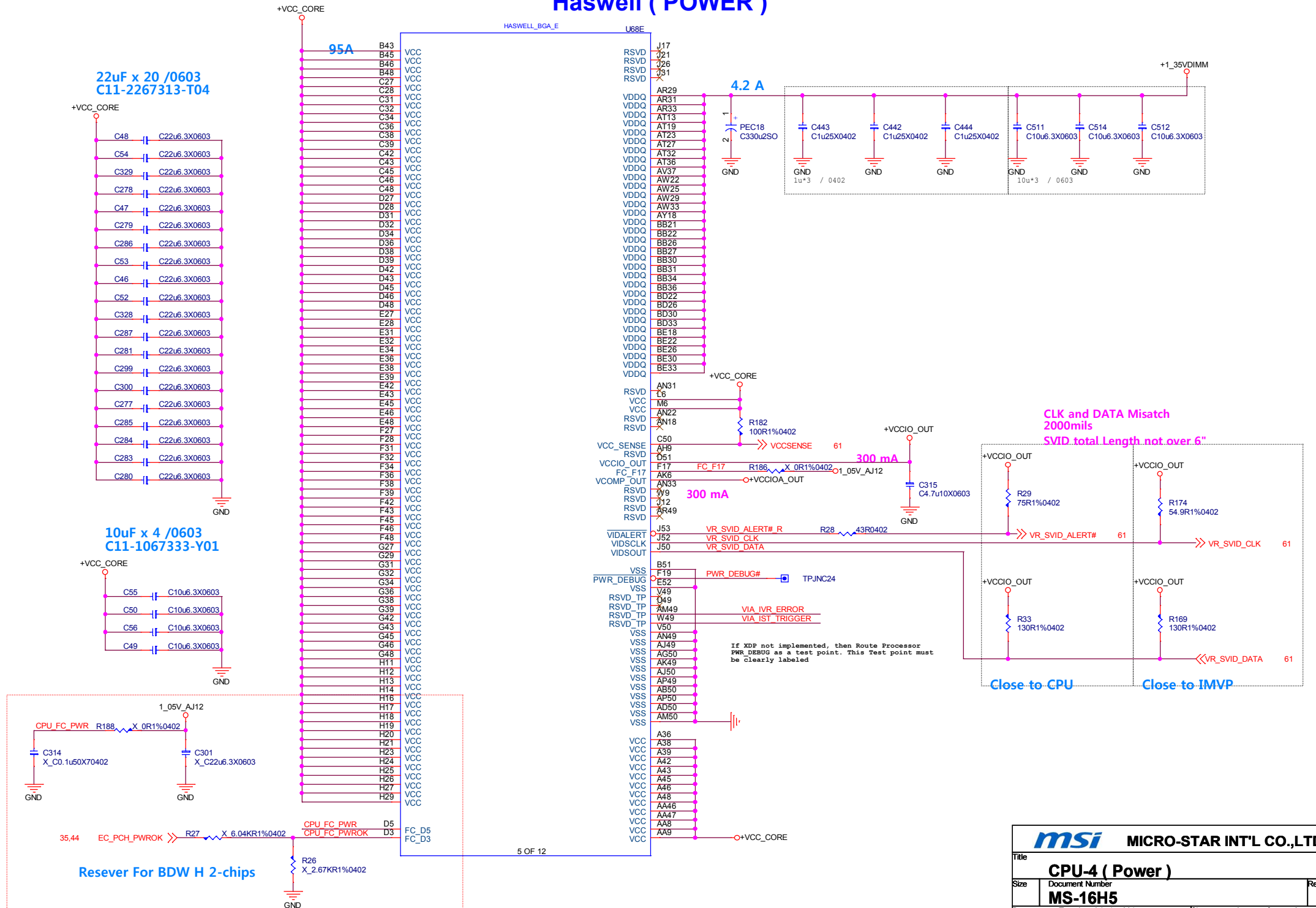
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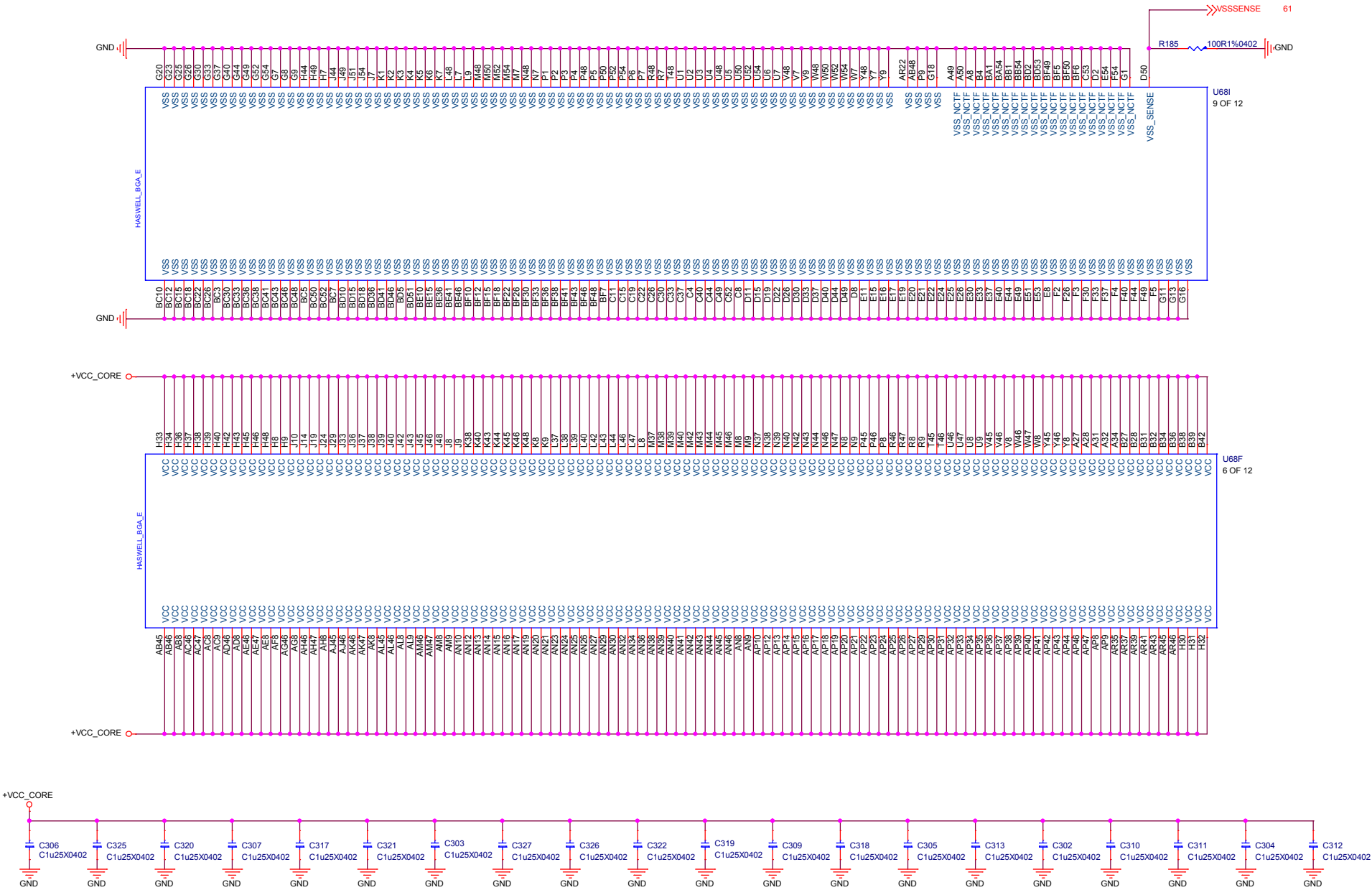
To eDP Panal



## Haswell ( POWER )

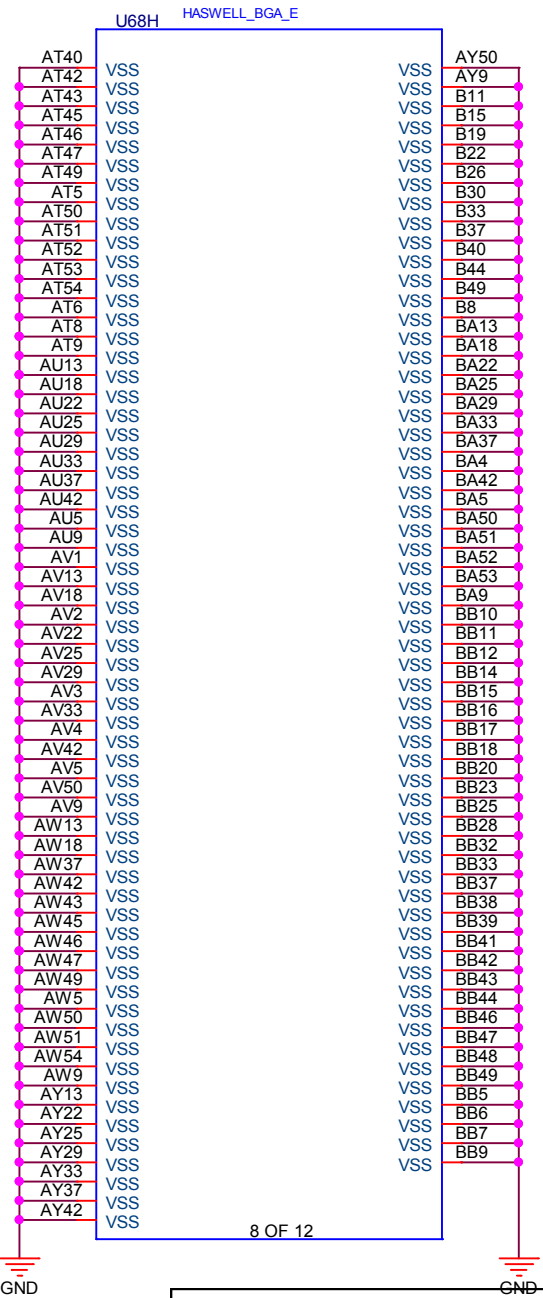
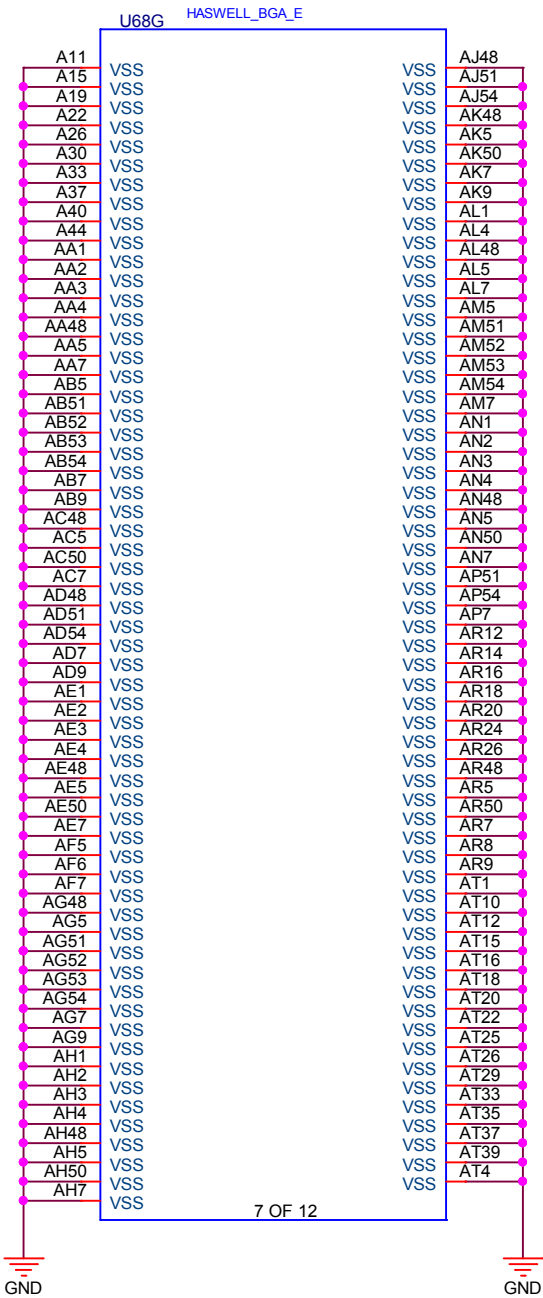



Haswell ( Power & GND )





Haswell ( GND )



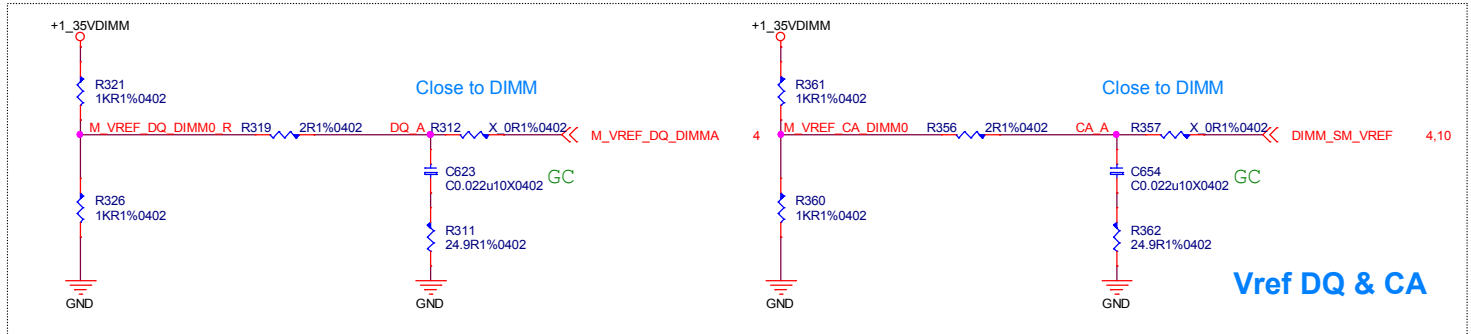
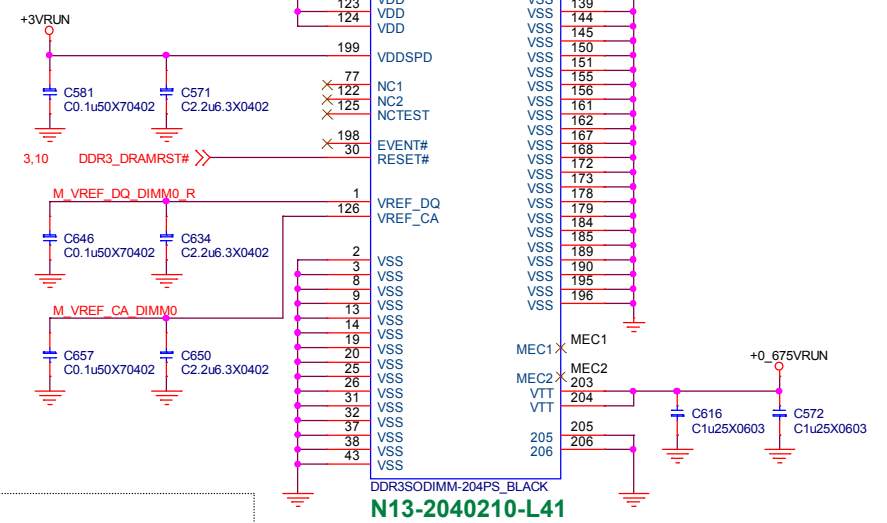
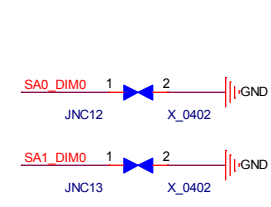
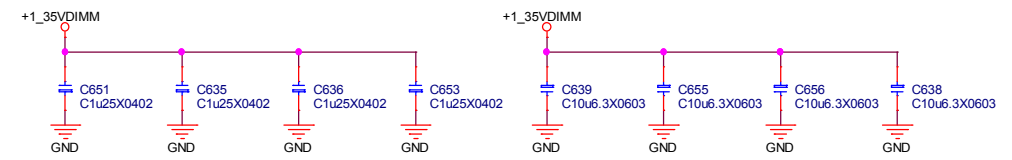
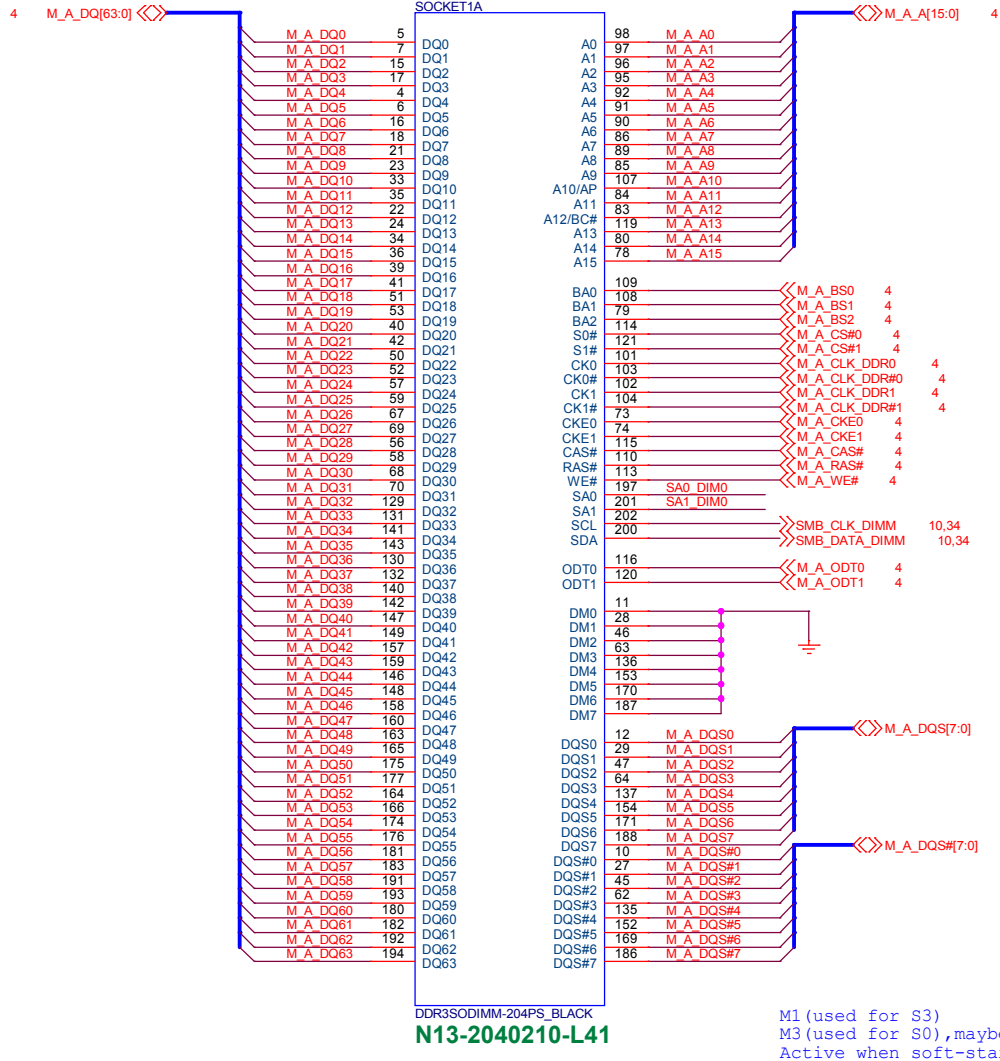


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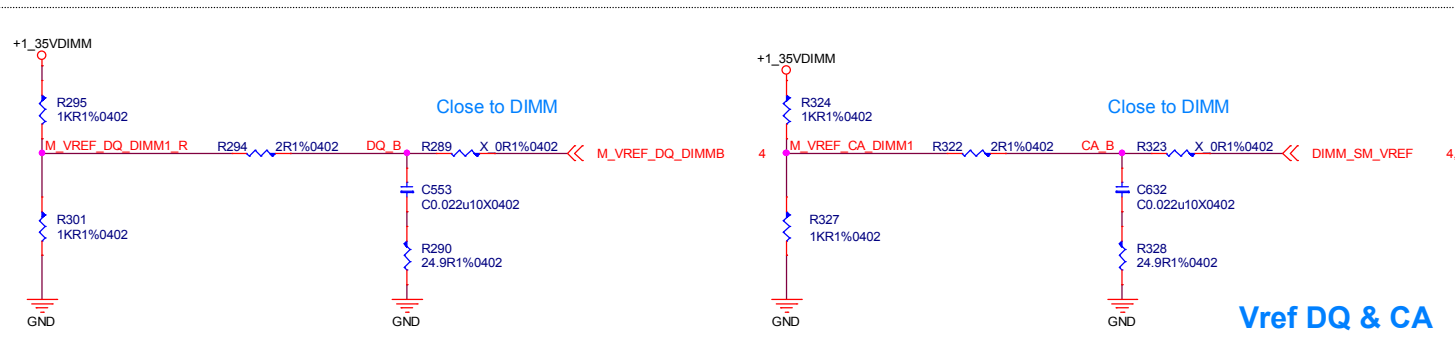
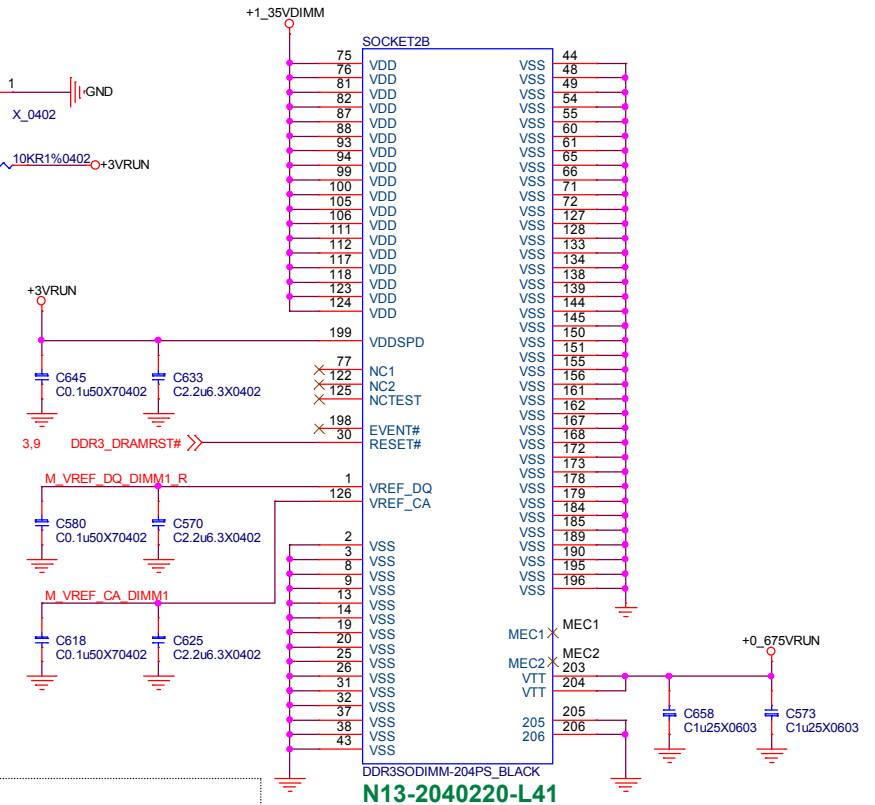
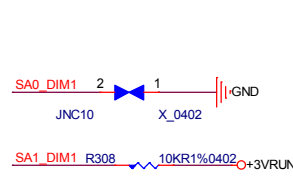
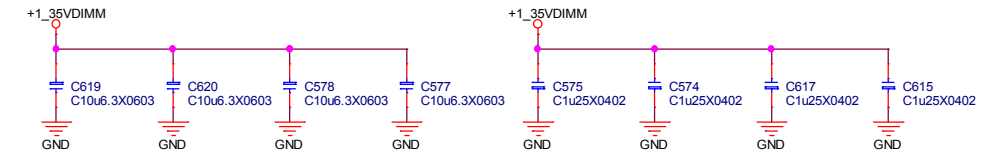
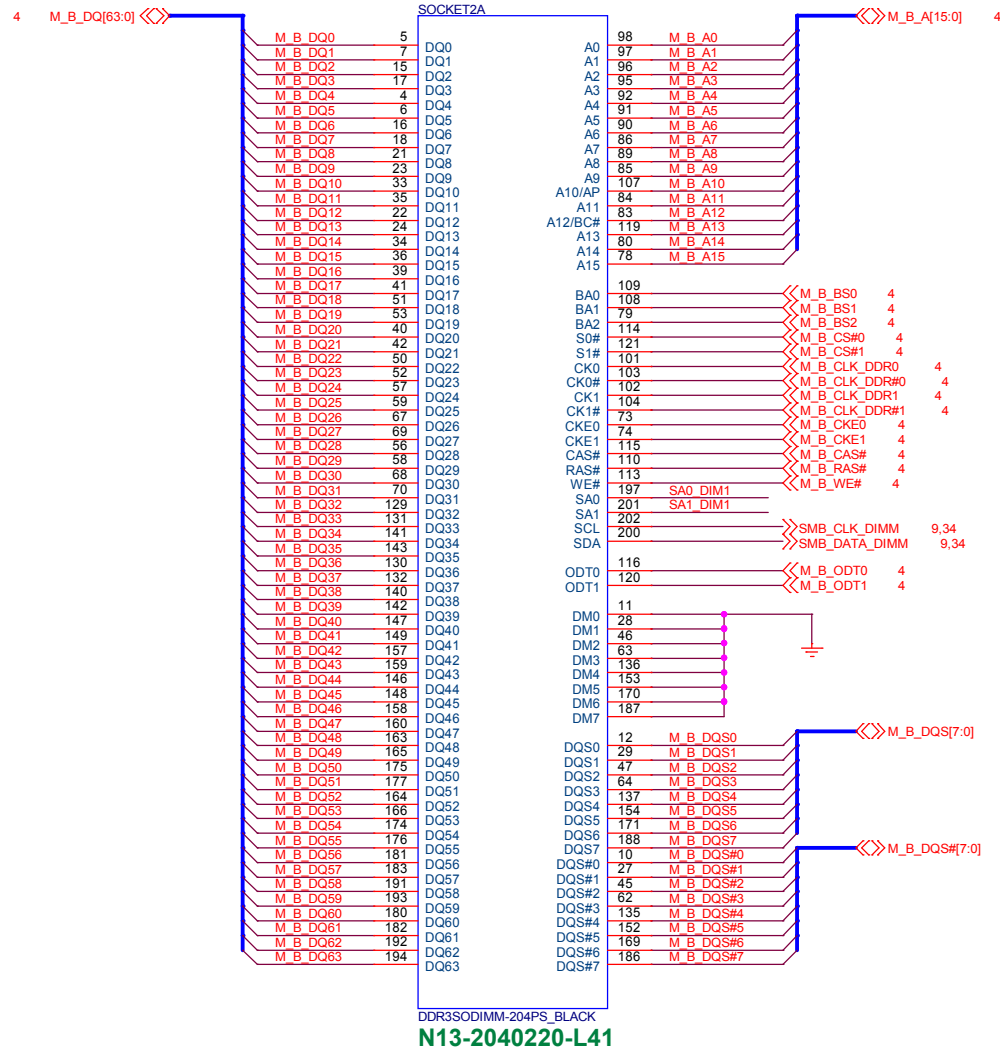
Title		
CPU-5 ( GND )		
Size	Document Number	Rev
	MS-16H5	1.1
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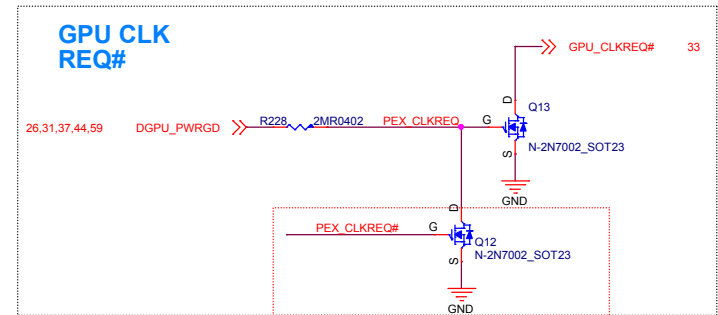
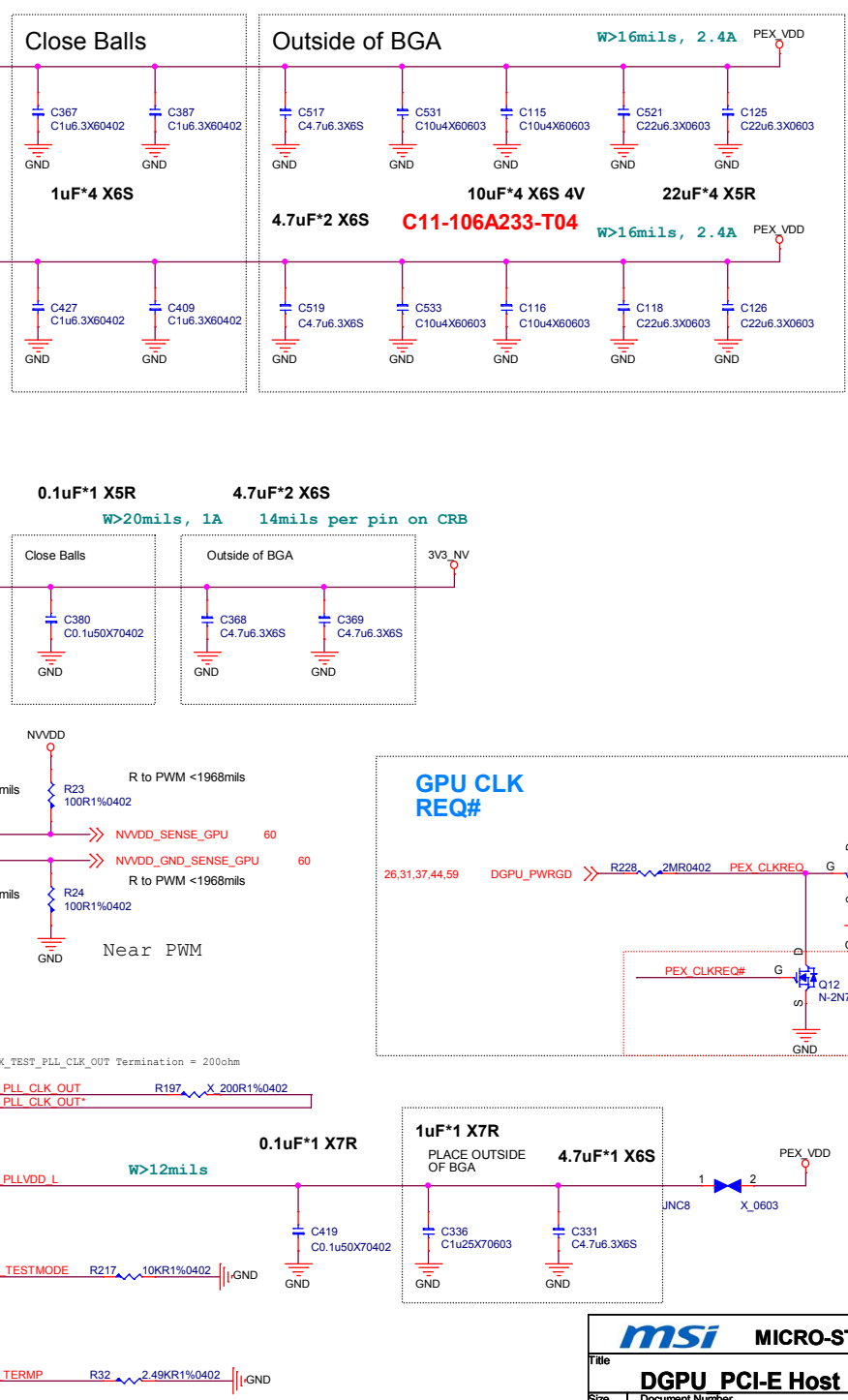
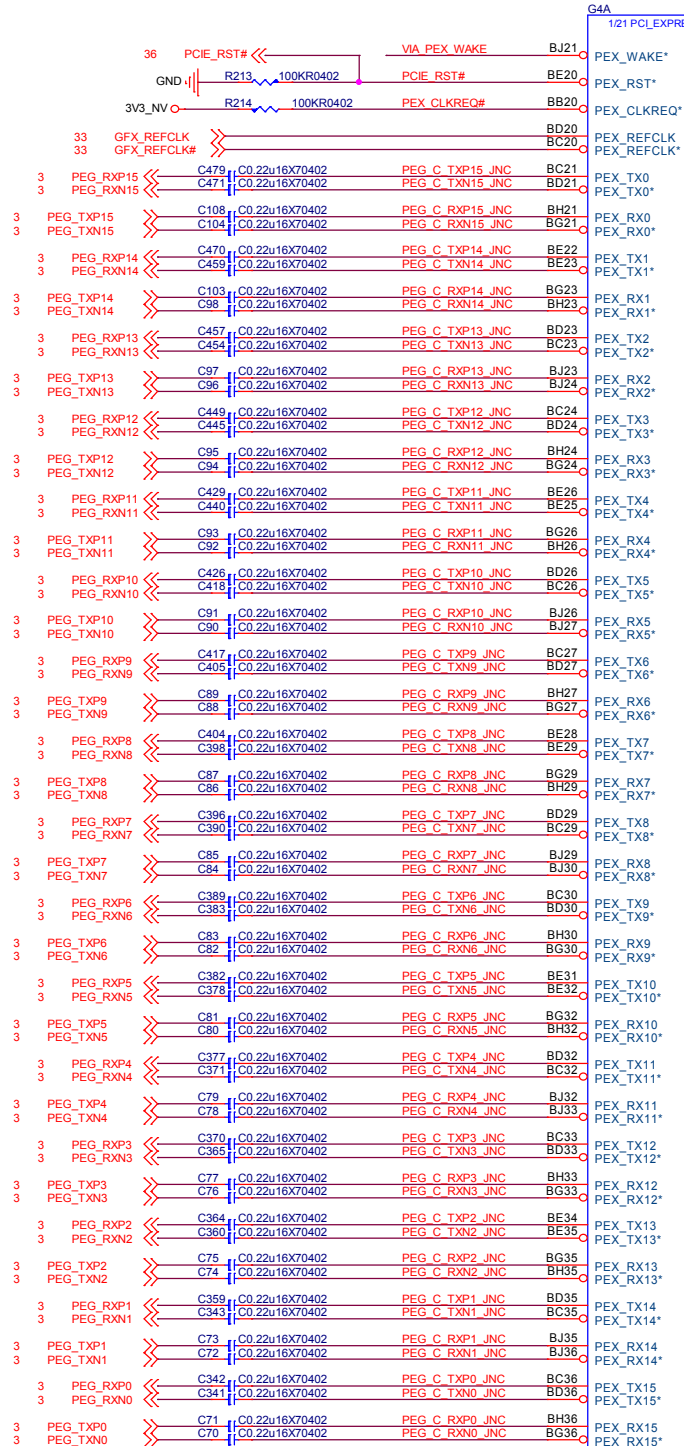
# SODIMM#A



## SODIMM#B

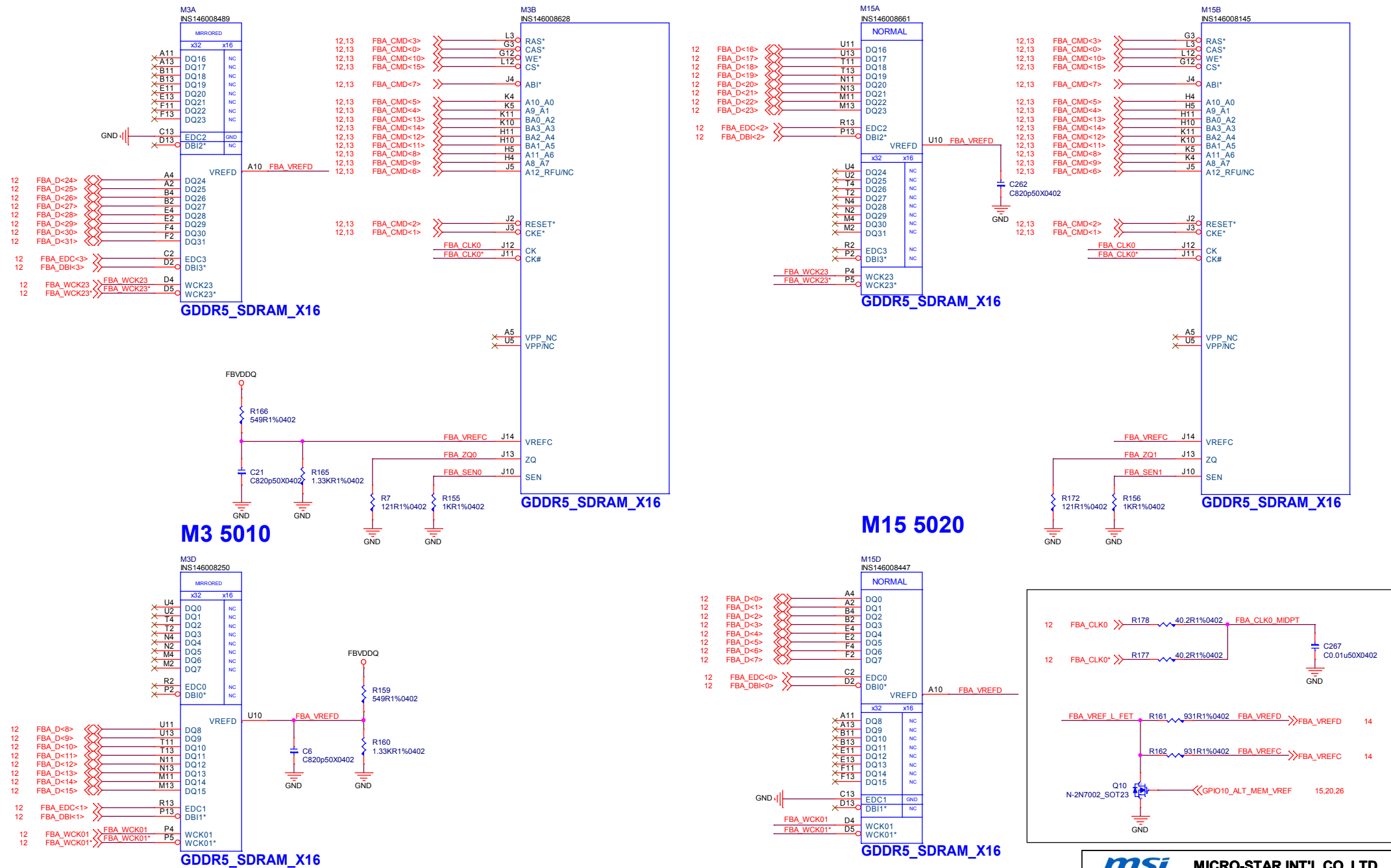


# GPU PCI EXPRESS



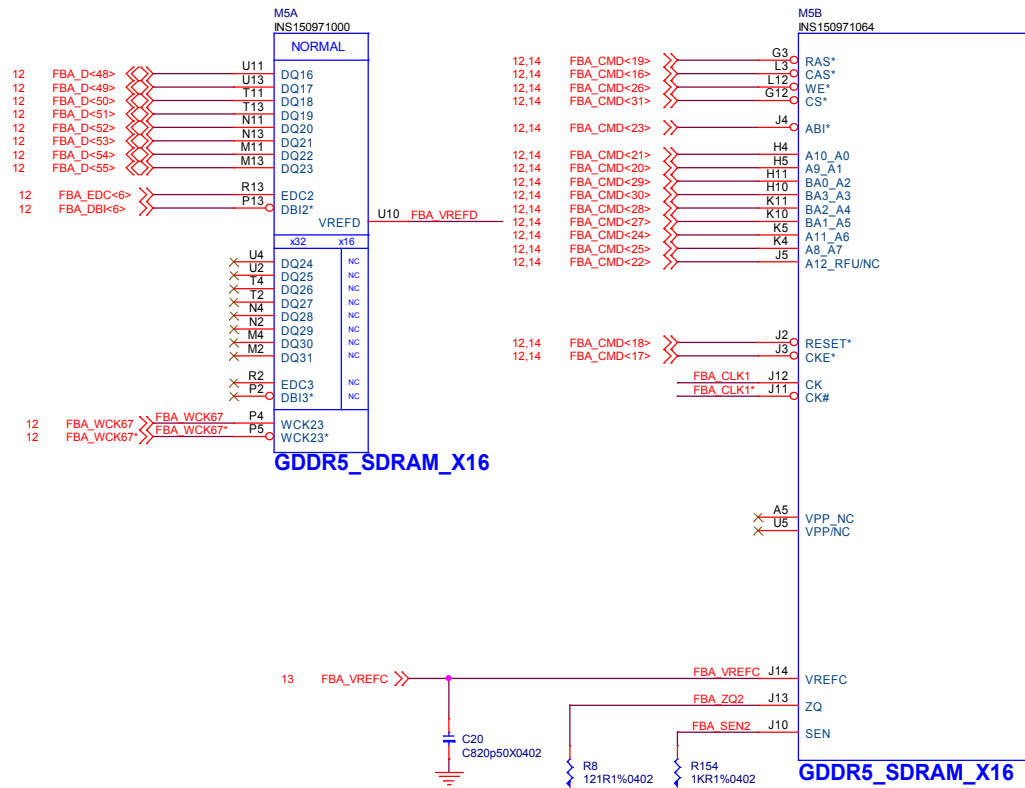


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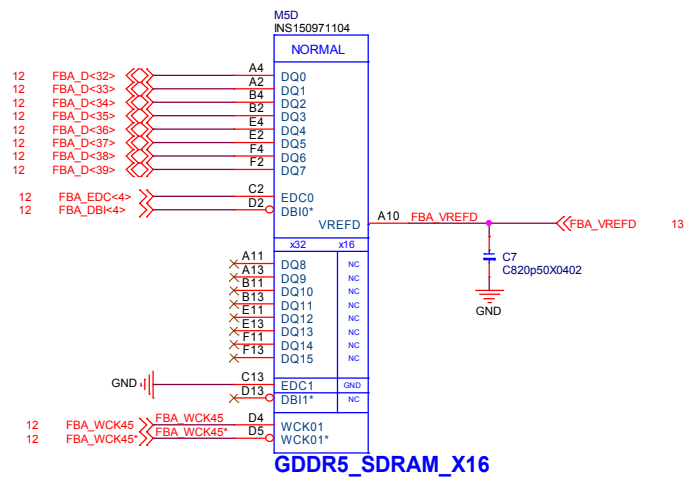




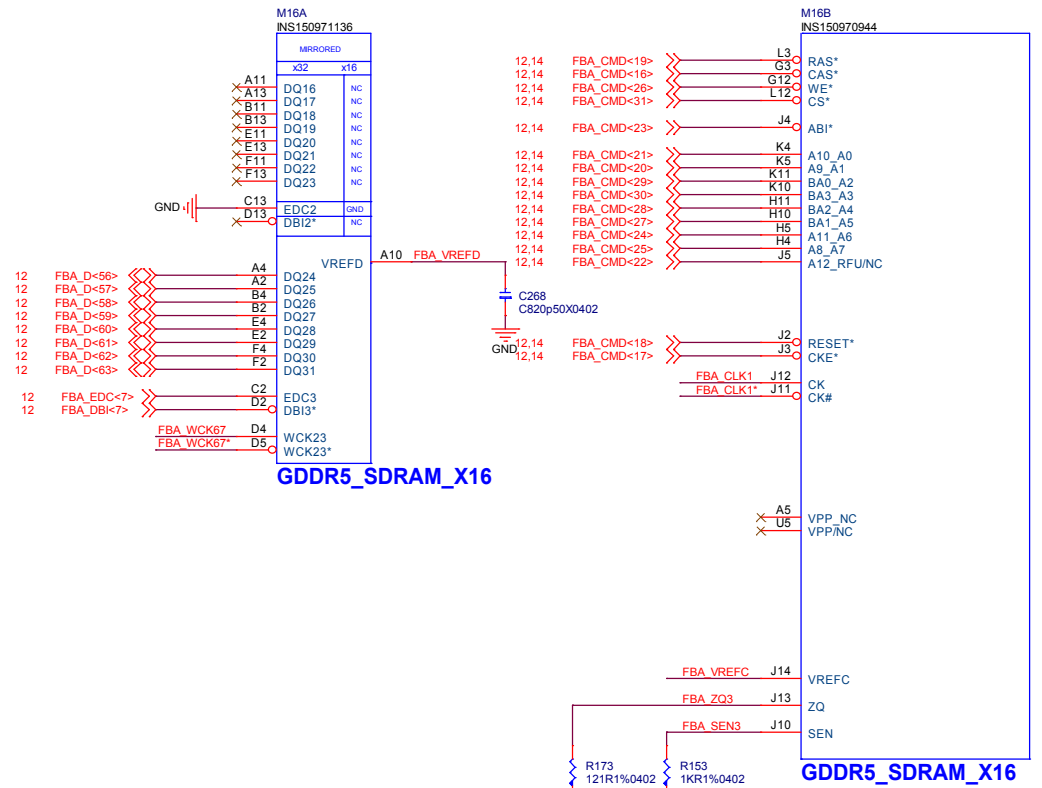
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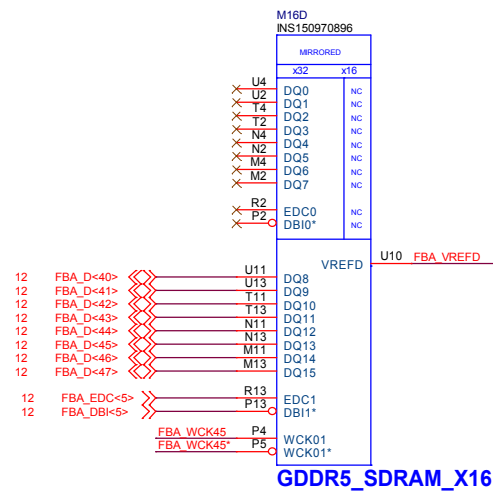
M5 5010



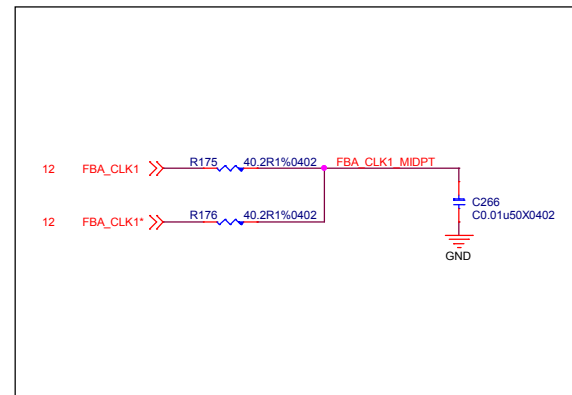
GDDR5\_SDRAM\_X16



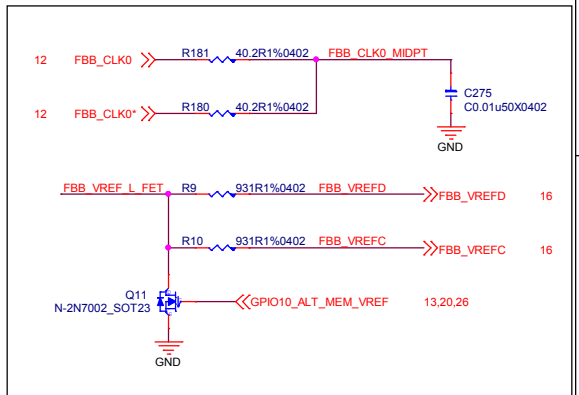
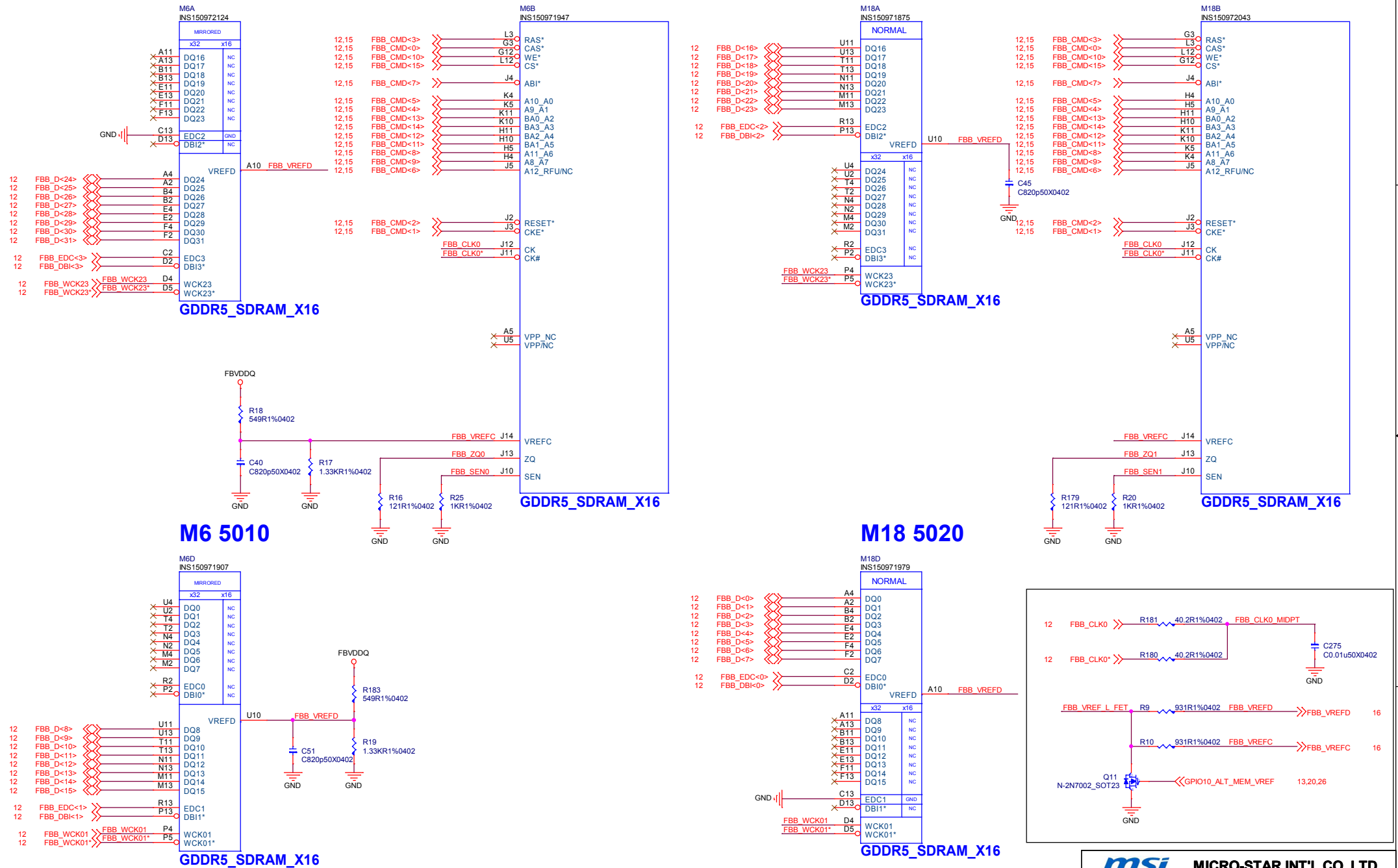
M16 5020



GDDR5\_SDRAM\_X16

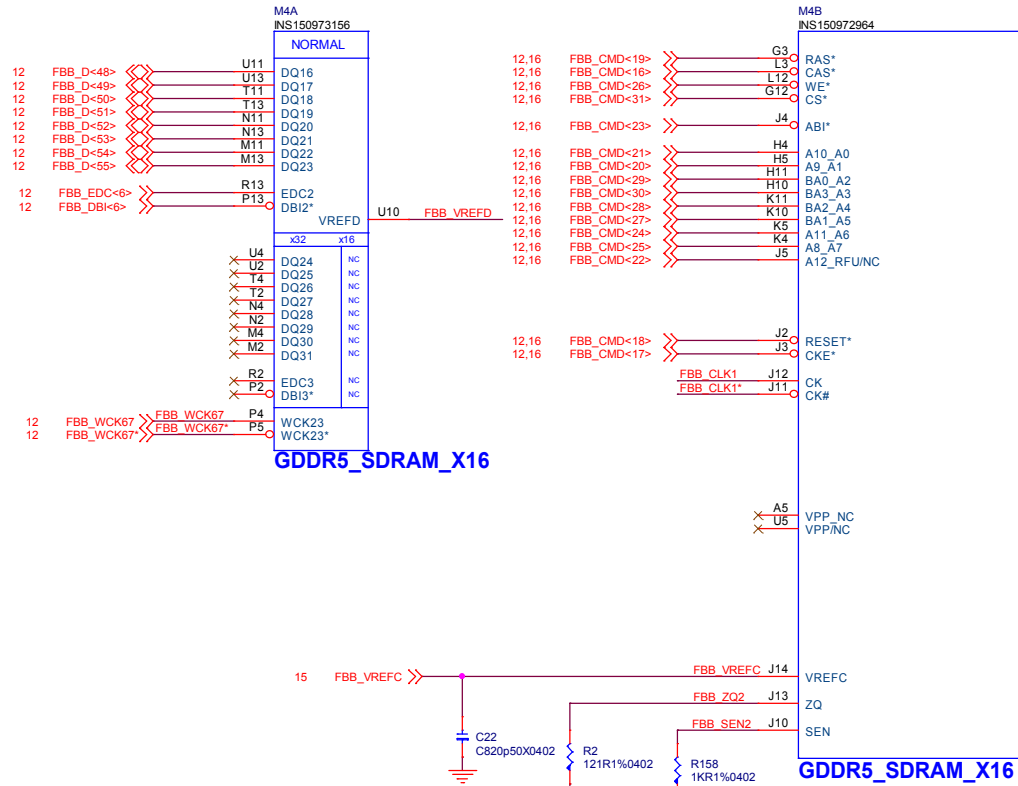


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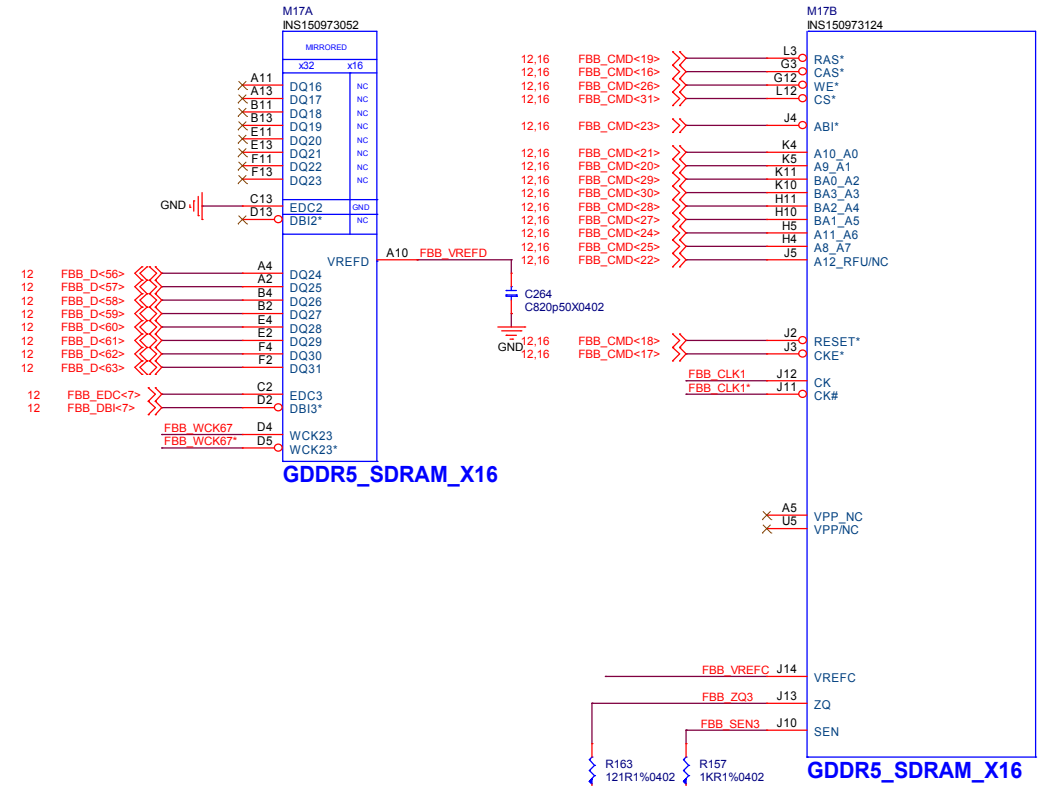
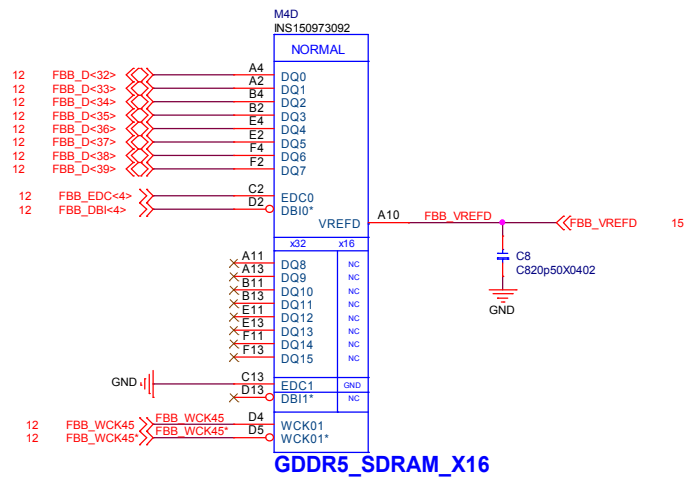




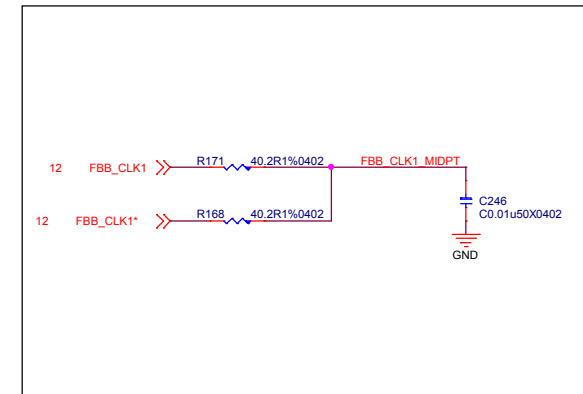
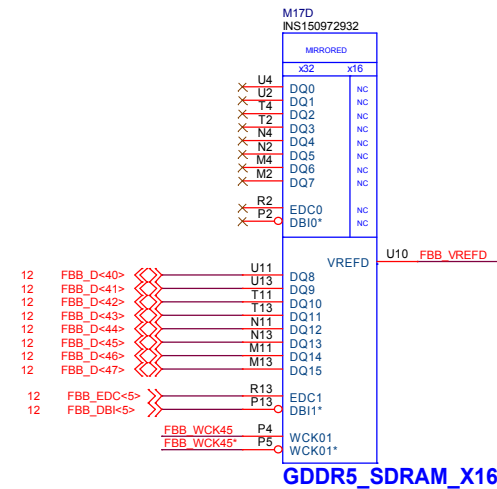
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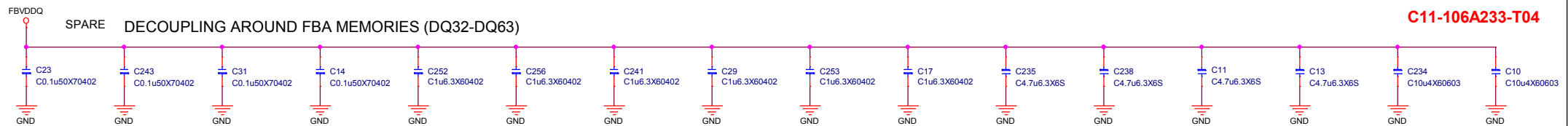
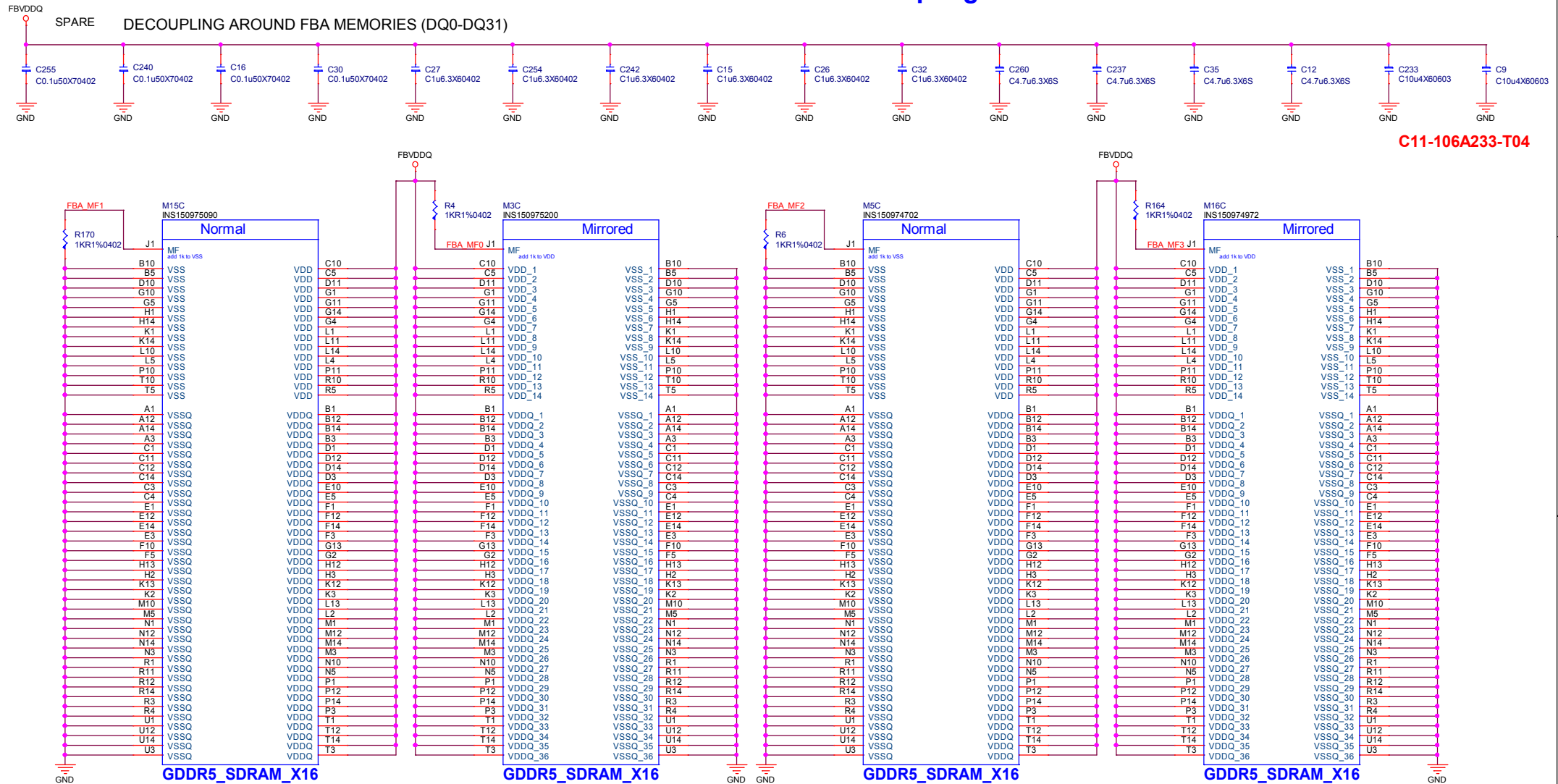
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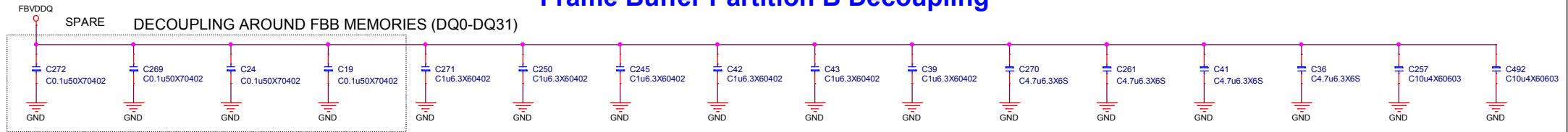
**M17 5020**



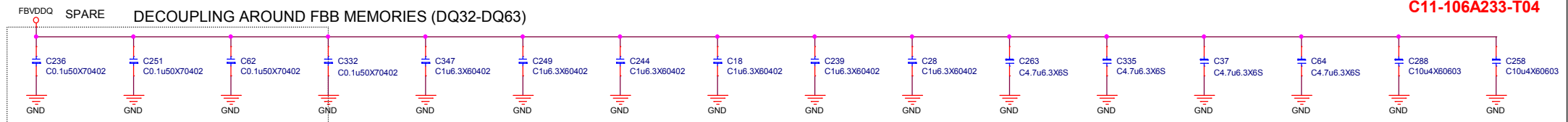
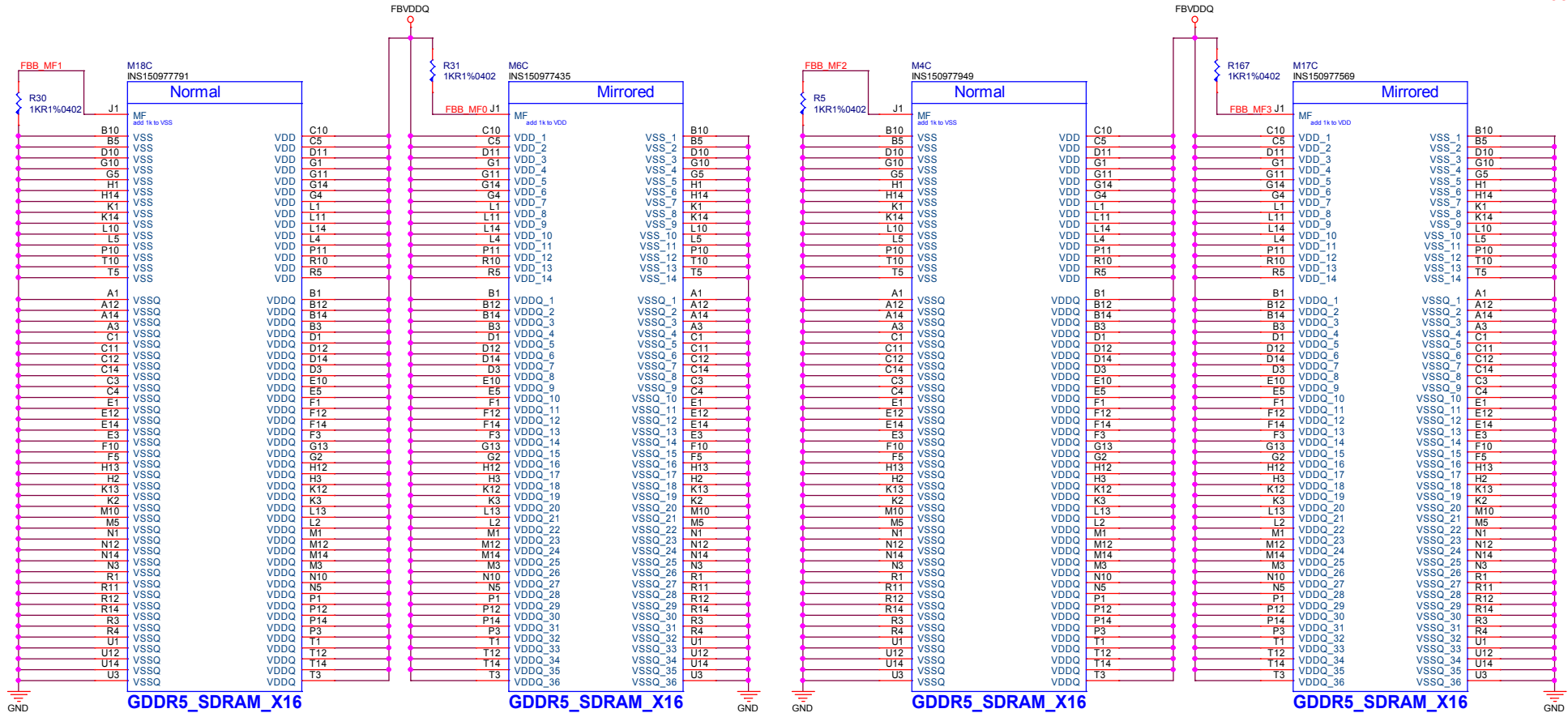
## Frame Buffer Partition A Decoupling



## Frame Buffer Partition B Decoupling

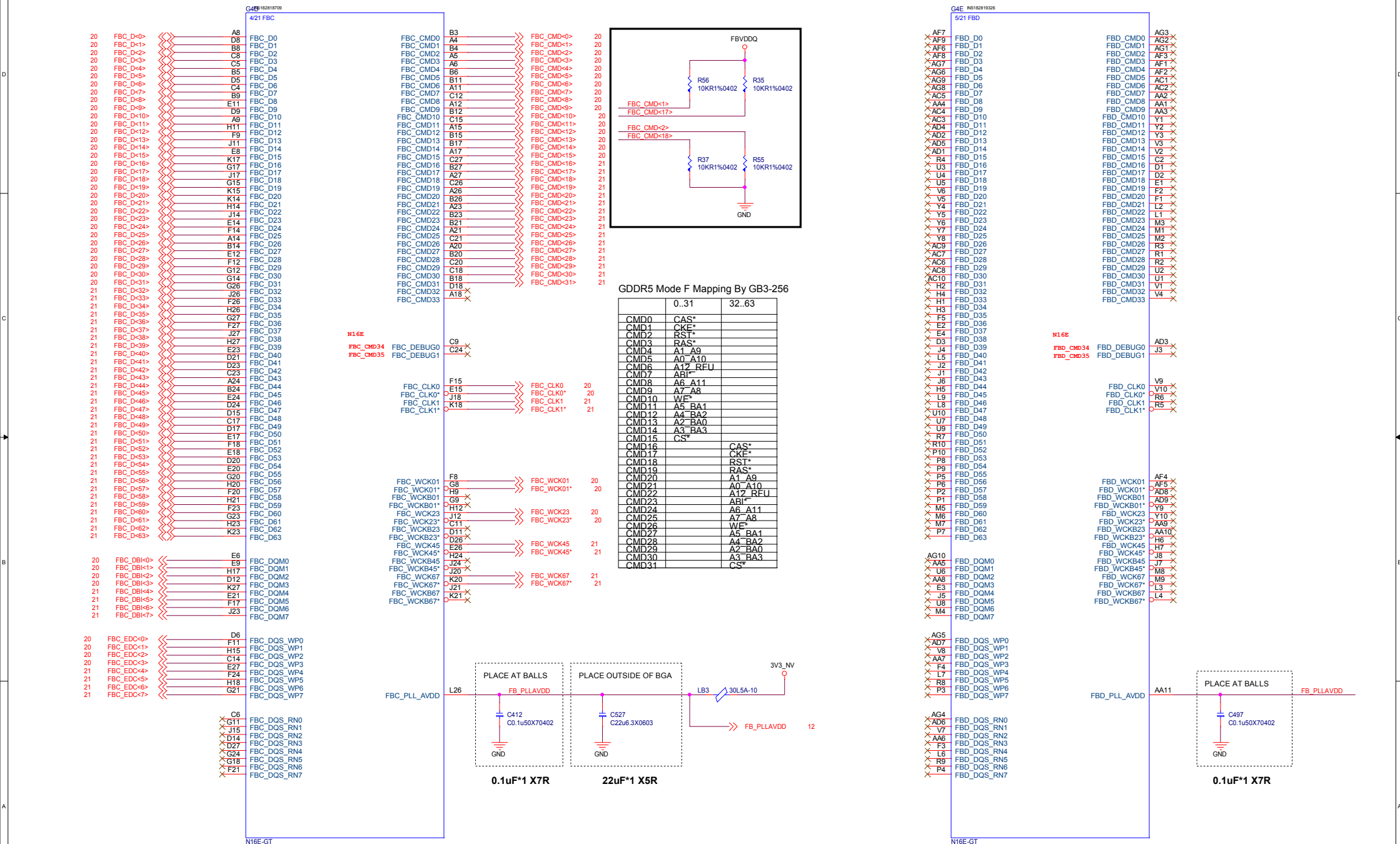


**C11-106A233-T04**

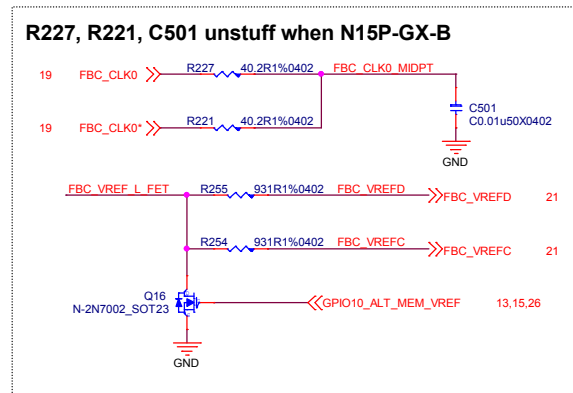
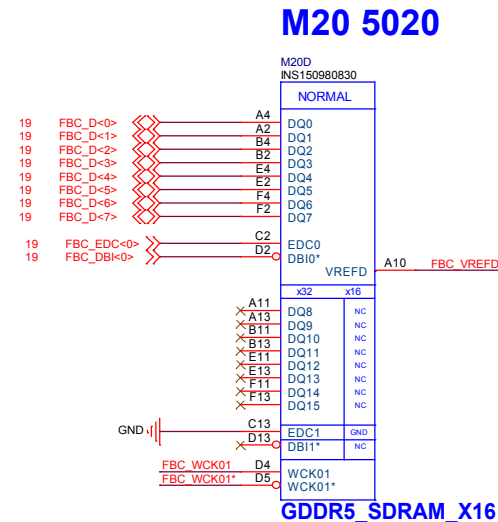
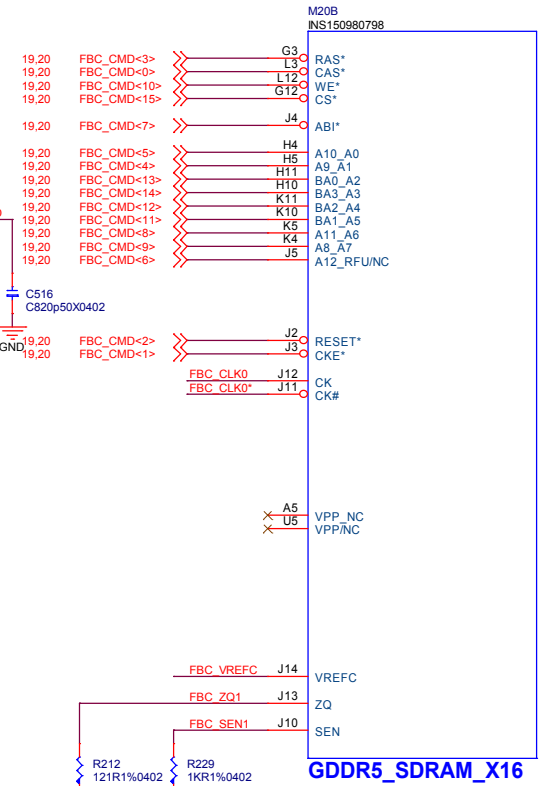


**C11-106A233-T04**

## GPU Frame Buffer Partition C/D

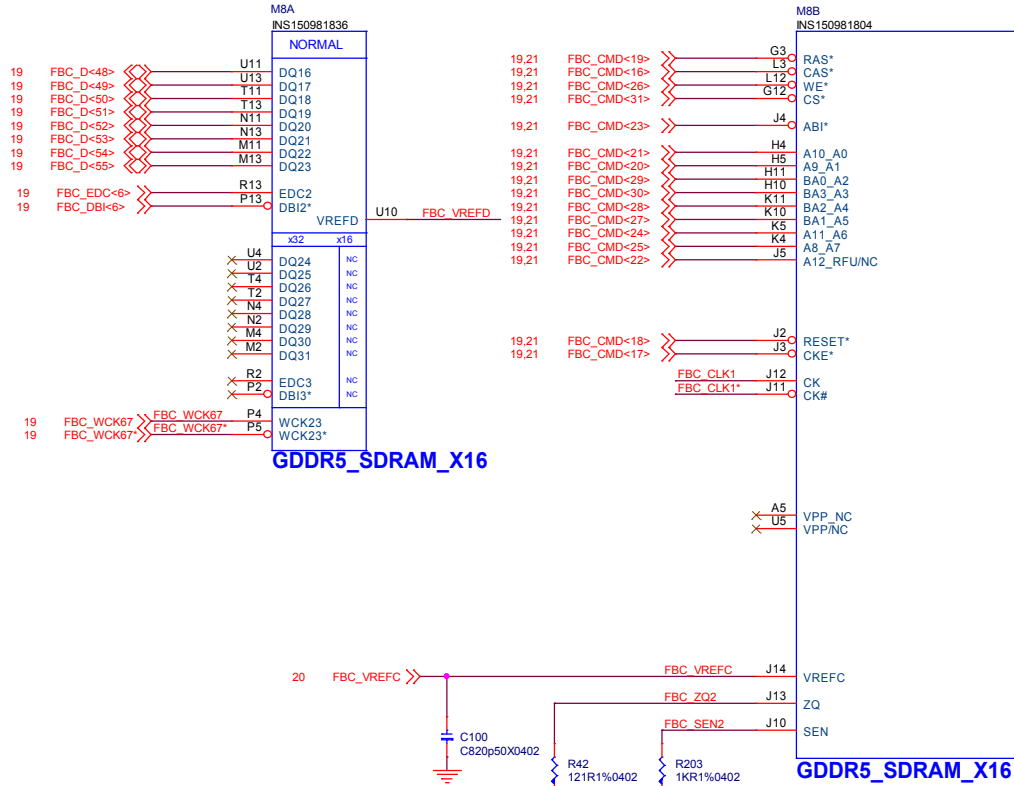


**(N16P-GX-B ALL unstuff)**

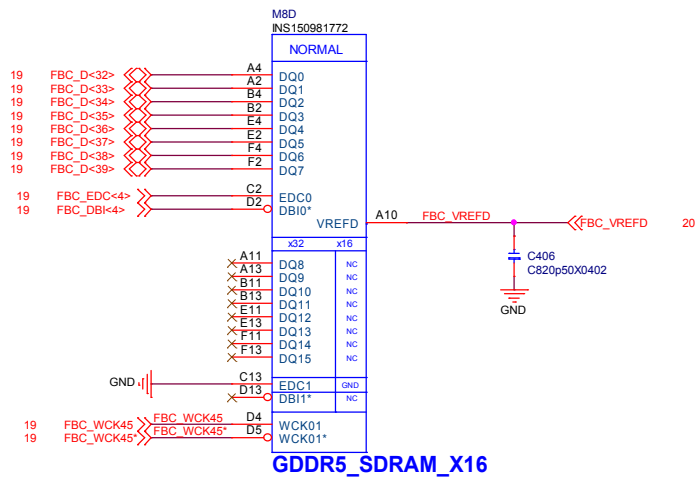


# DGPU\_GDDR5 FrameBuffer C1

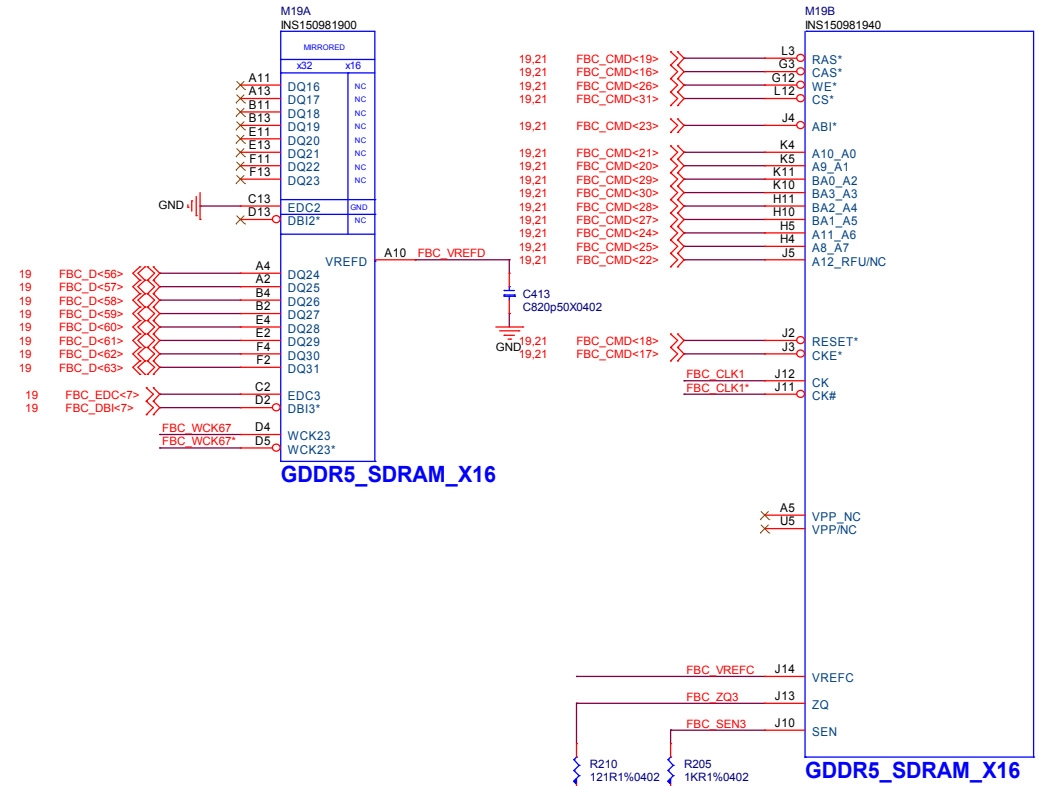
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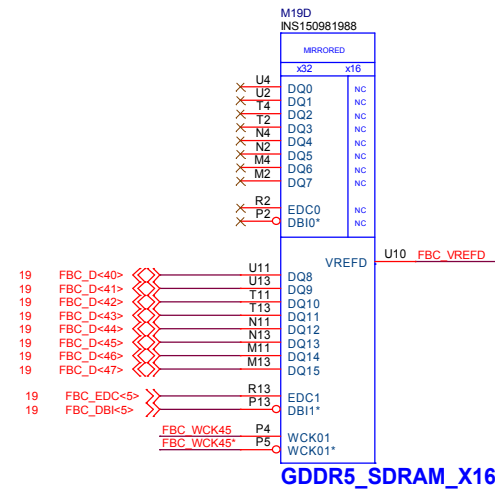
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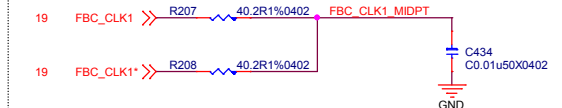


M19 5020



GDDR5\_SDRAM\_X16

R227, R221, C501 unstuff when N15P-GX-B



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DGPU\_GDDR5 FrameBuffer C

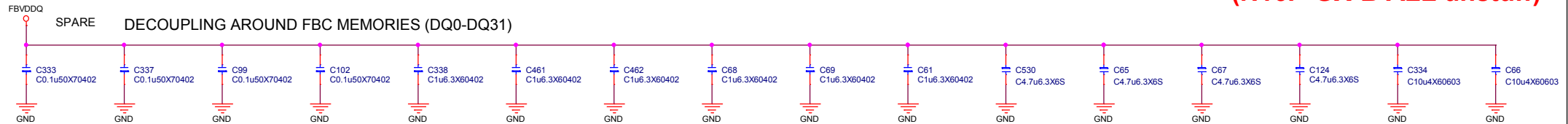
MS-16H5

Rev 1.1

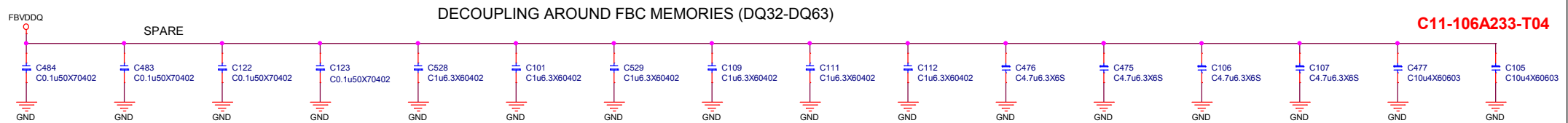
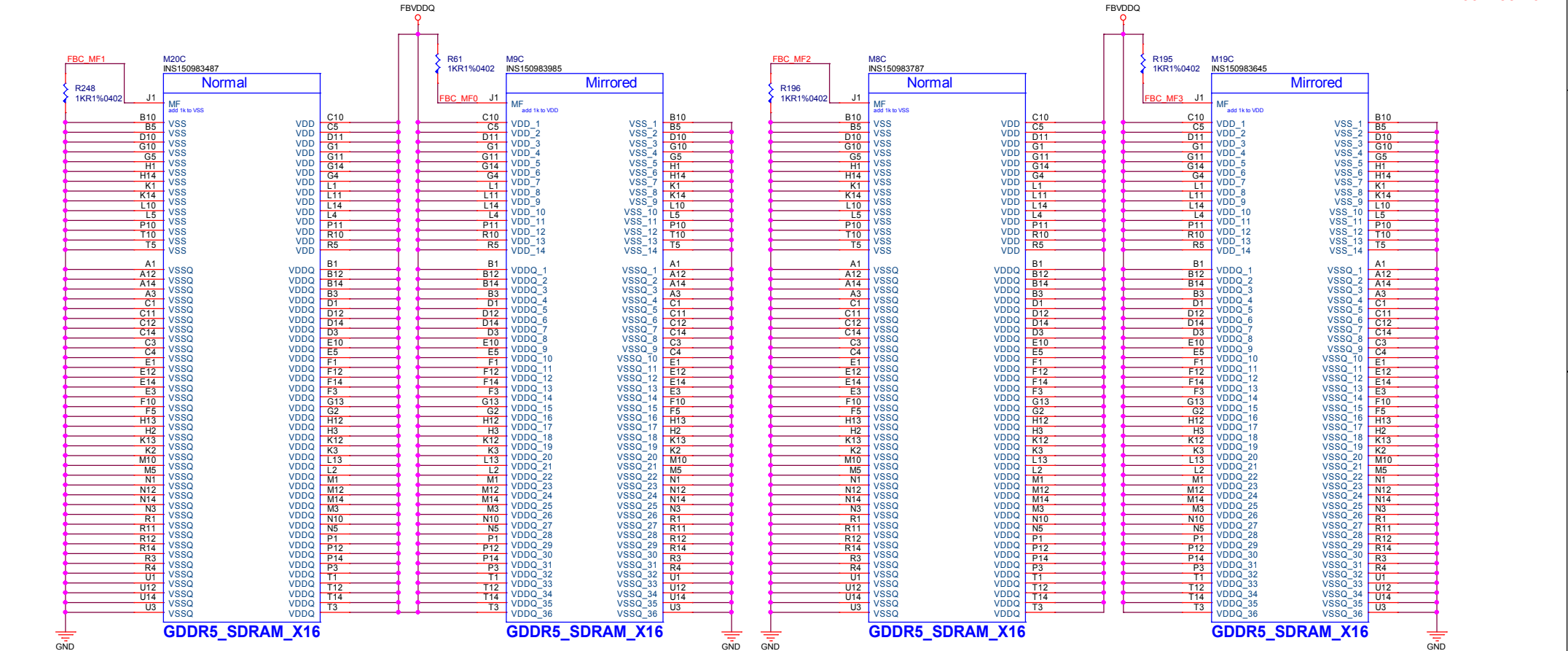
Date: Tuesday, July 15, 2014 Sheet 21 of 72

# Frame Buffer Partition C Decoupling

(N16P-GX-B ALL unstuff)



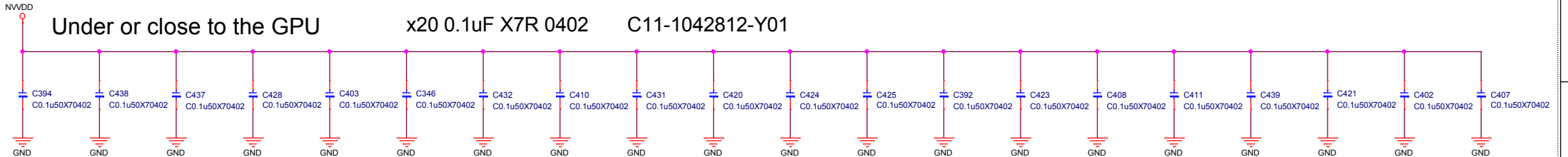
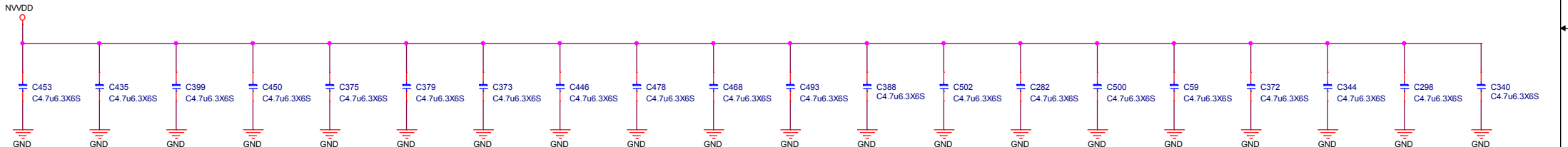
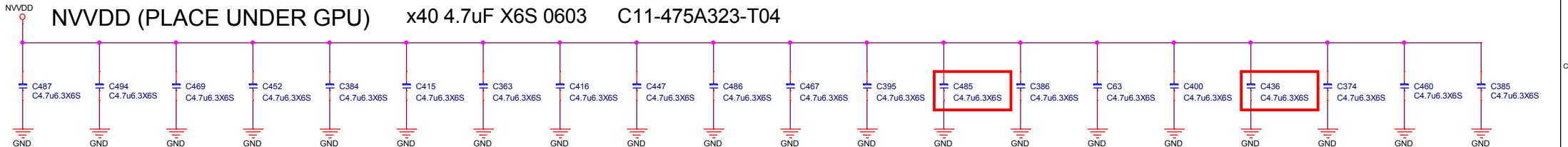
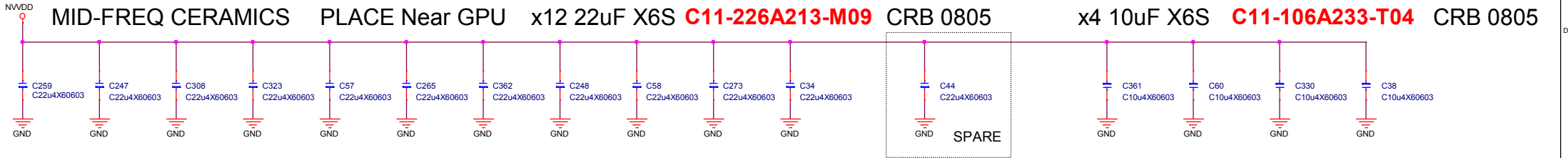
C11-106A233-T04



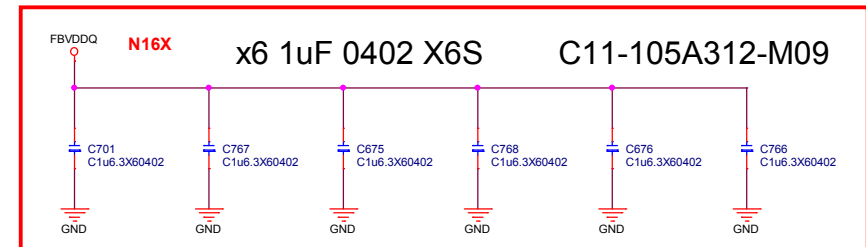
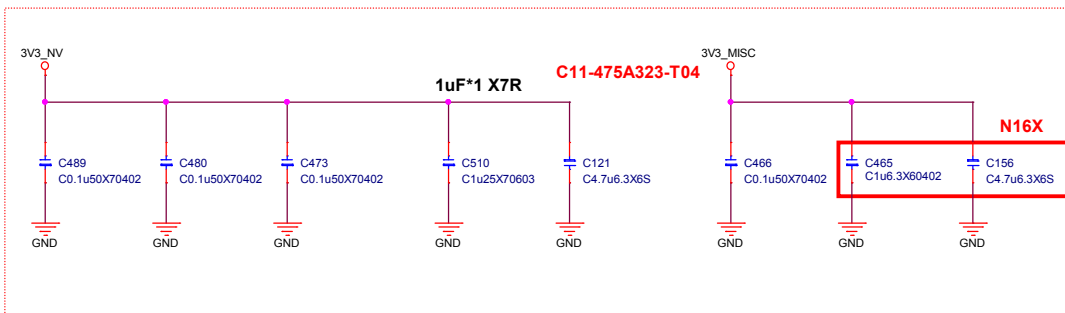
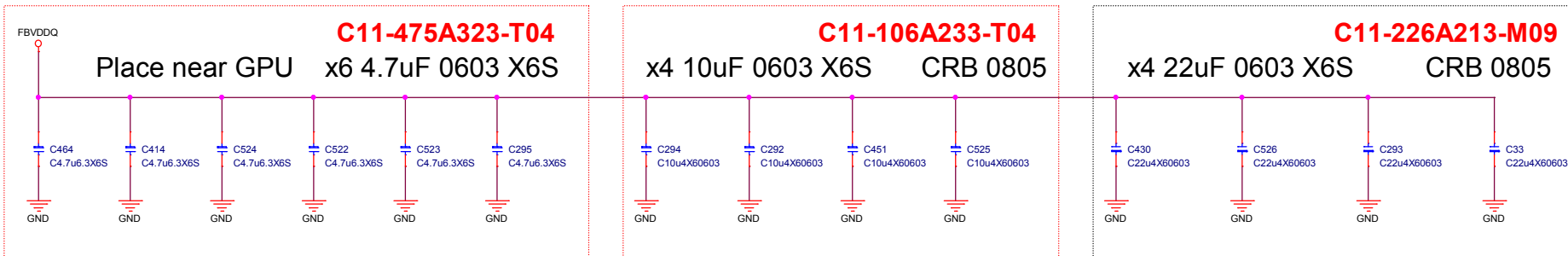
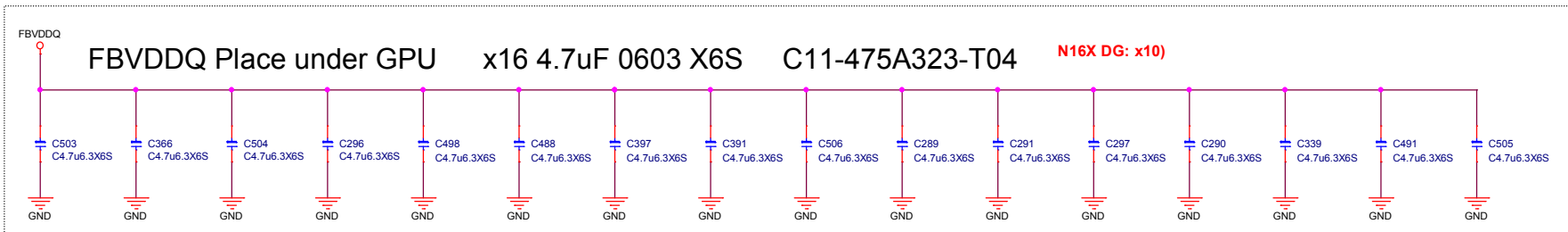
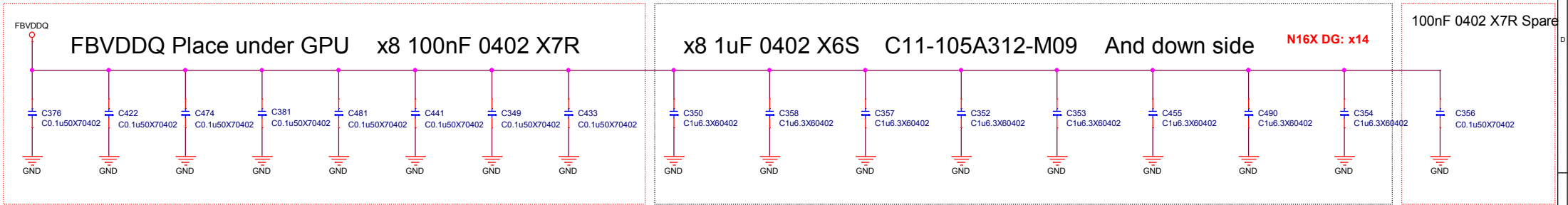
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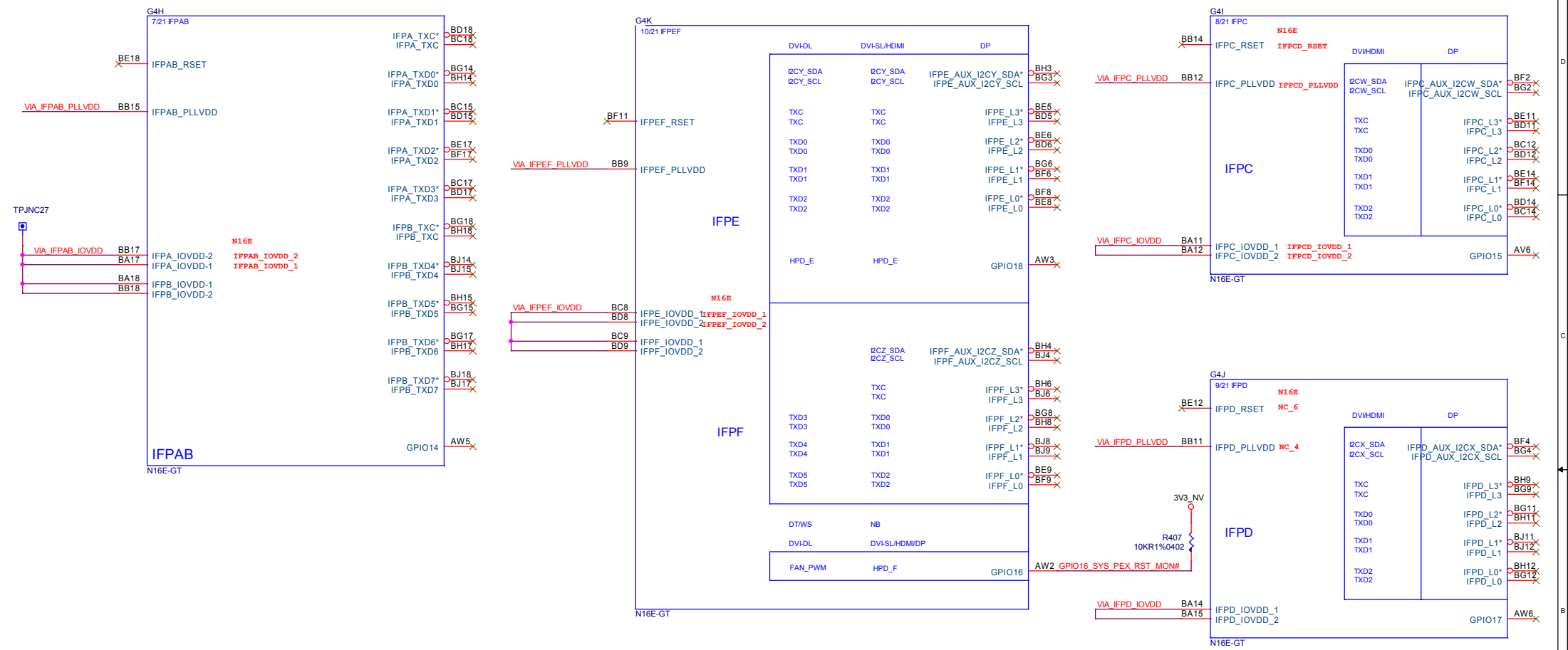
GPU DECOUPLING A



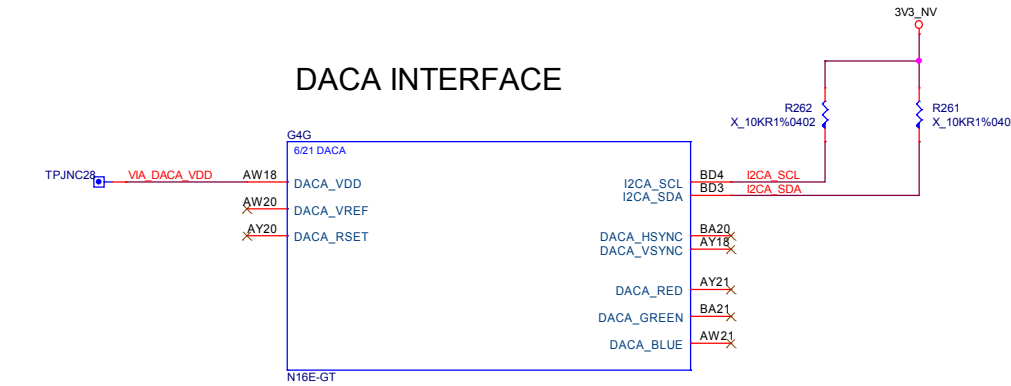
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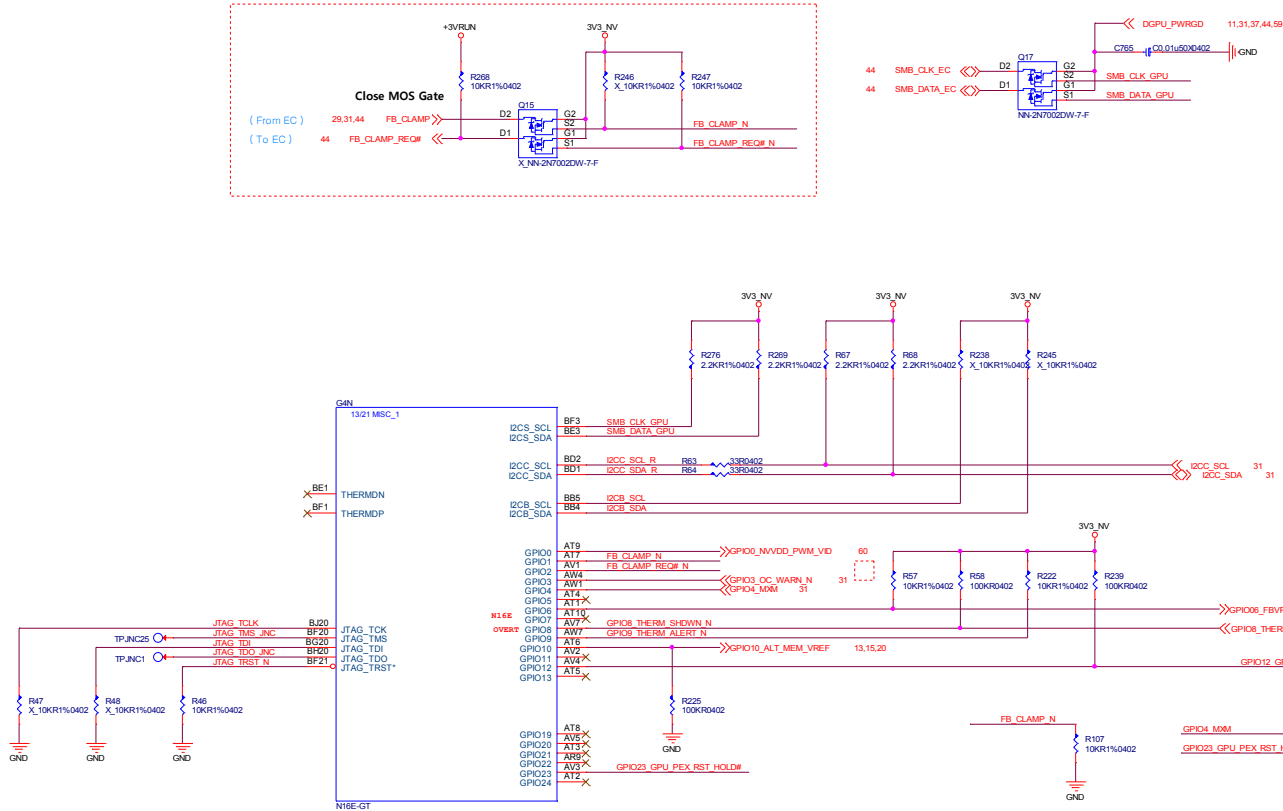
DACA,Display IF



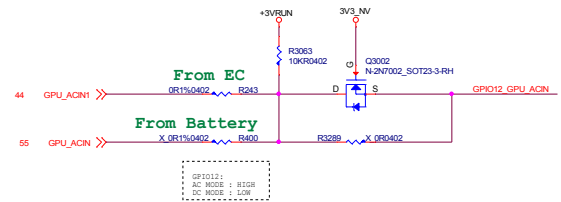
DACA INTERFACE



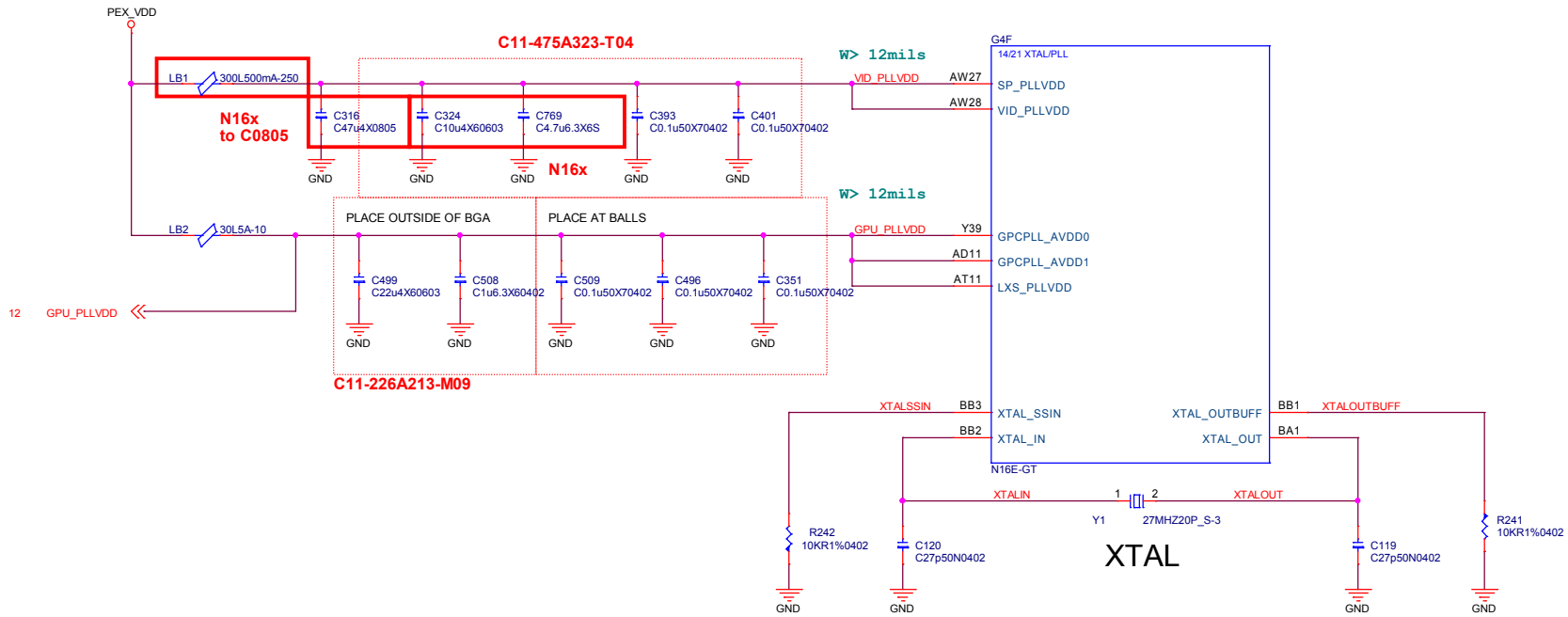
## DGPU GPIO, I2C



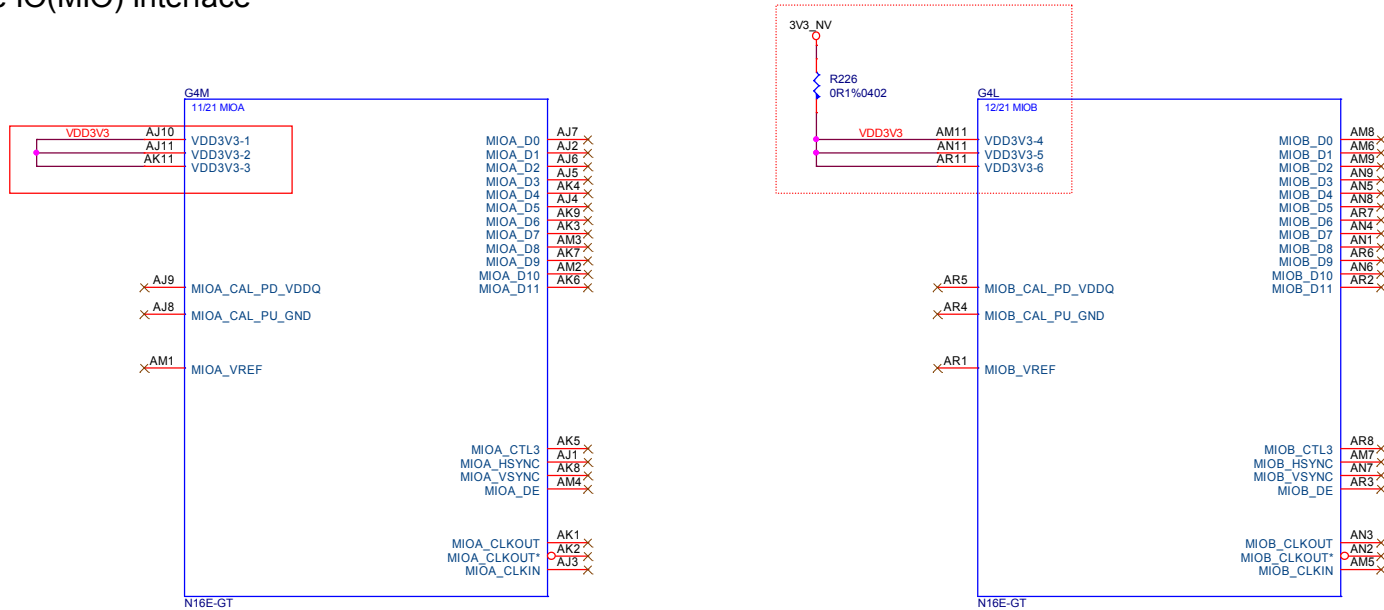
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GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO3	OC_WARN	I	Over current throttling	10K pull-up to 3V3_AON
GPIO4	3V3_MAIN_EN	O	GPU POWER Sequencing for GC6 2.0	10K pull-up to 3V3_AON
GPIO5	RESERVED			
GPIO6	PSI	O	Phase shedding	
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	HPD_F	I	Hot Plug Detect for IPPDF	
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overload input	100K pull-up to 3V3_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IPFAB	
GPIO15	HPD_C	I	Hot Plug Detect for IPFC	
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 3V3_AON
GPIO17	HPD_D	I	Hot Plug Detect for IPFD	
GPIO18	HPD_E	I	Hot Plug Detect for IPFE	
GPIO19	3Dvision	O	3D Vision L/R signal	100K pull-down
GPIO20	RESERVED			
GPIO21	SLI_RASTER_SYNC	I	SLi Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLi Swap Ready	1K pull-up to 3V3_AON
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIe self-reset control	10K pull-up to 3V3_AON
GPIO24	MEM_VDD_CTL	O	Memory VDD VID	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_B	I	Hot Plug Detect for IPFB	
OVERT	OVERT (OVERT#)	I/O	Catastrophic Over Temperature	100K pull-up to 3V3_AON



## DGPU MIO & XTAL



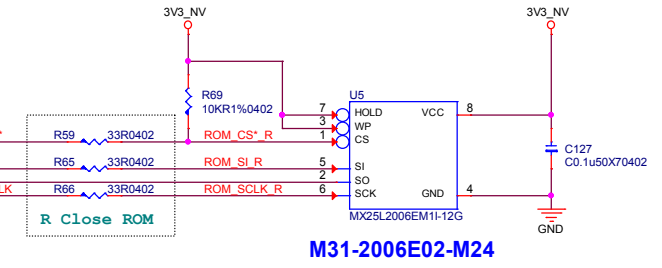
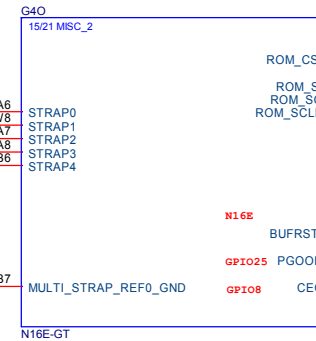
## Multi-use IO(MIO) Interface



# ROM, MULTI-LEVEL STRAPS

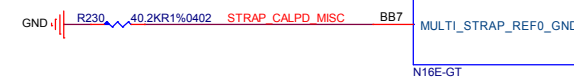
	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU

STRAP0 BA6  
STRAP1 AW8  
STRAP2 BA7  
STRAP3 BA8  
STRAP4 BB6



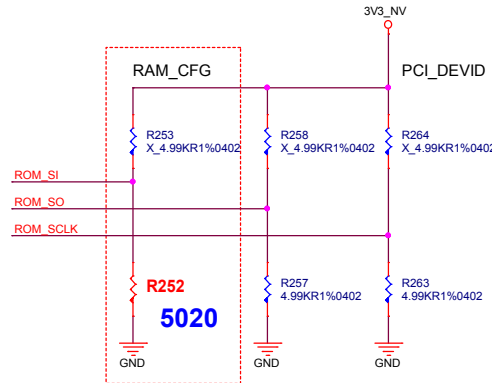
M31-2006E02-M24

ROM_SI10K	Hynix	V_TOP1	5010	5020
R11-0103T12-W08	M12-5GC2H05-H23	M12-5GC2H05-H23		
X_10KR1%0402	X_H5GC2H24BFR-T2C	X_H5GC2H24BFR-T2C		

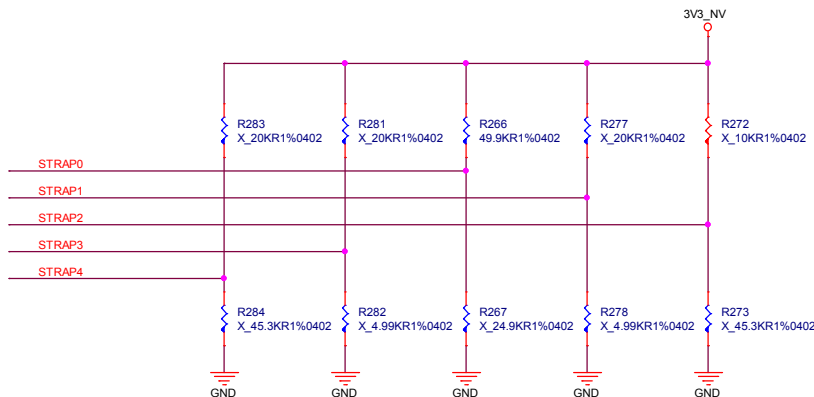


ROM_SI5K	Samsung	V_TOP2	5010	5020
R11-4991T12-W08	M12-2032585-S02	M12-2032585-S02		
X_5KR1%0402	X_K4G20325FD-FC03	X_K4G20325FD-FC03		

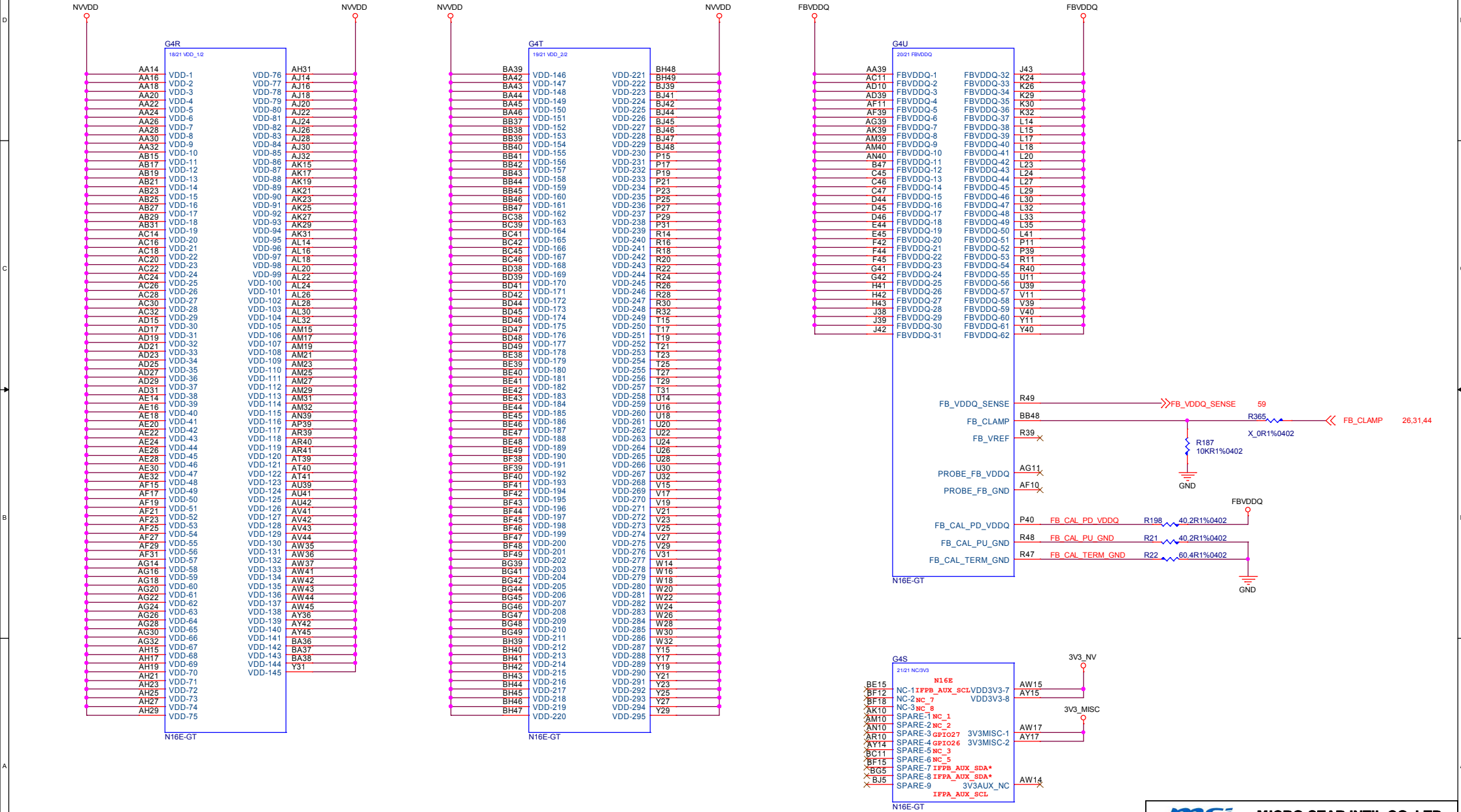
**GDDR5 Parts**  
5010 : M4 , M3 , M5 , M6 , M8 , M9  
5020 : M17, M15, M16, M18, M19, M20



	N16E-GT ES		N16E-GT QS	
ROM_SI	35K PD	Hynix 128x16bit	10K PD	Hynix 128x16bit
	45K PD	Samsung 128x16bit	5K PD	Samsung 128x16bit
ROM_SO	5K PD			
ROM_SCLK	5K PD			
STRAP0	50K PU 3V3_AON			
STRAP1	Reserved			
STRAP2	Reserved			
STRAP3	Reserved			
STRAP4	Reserved			

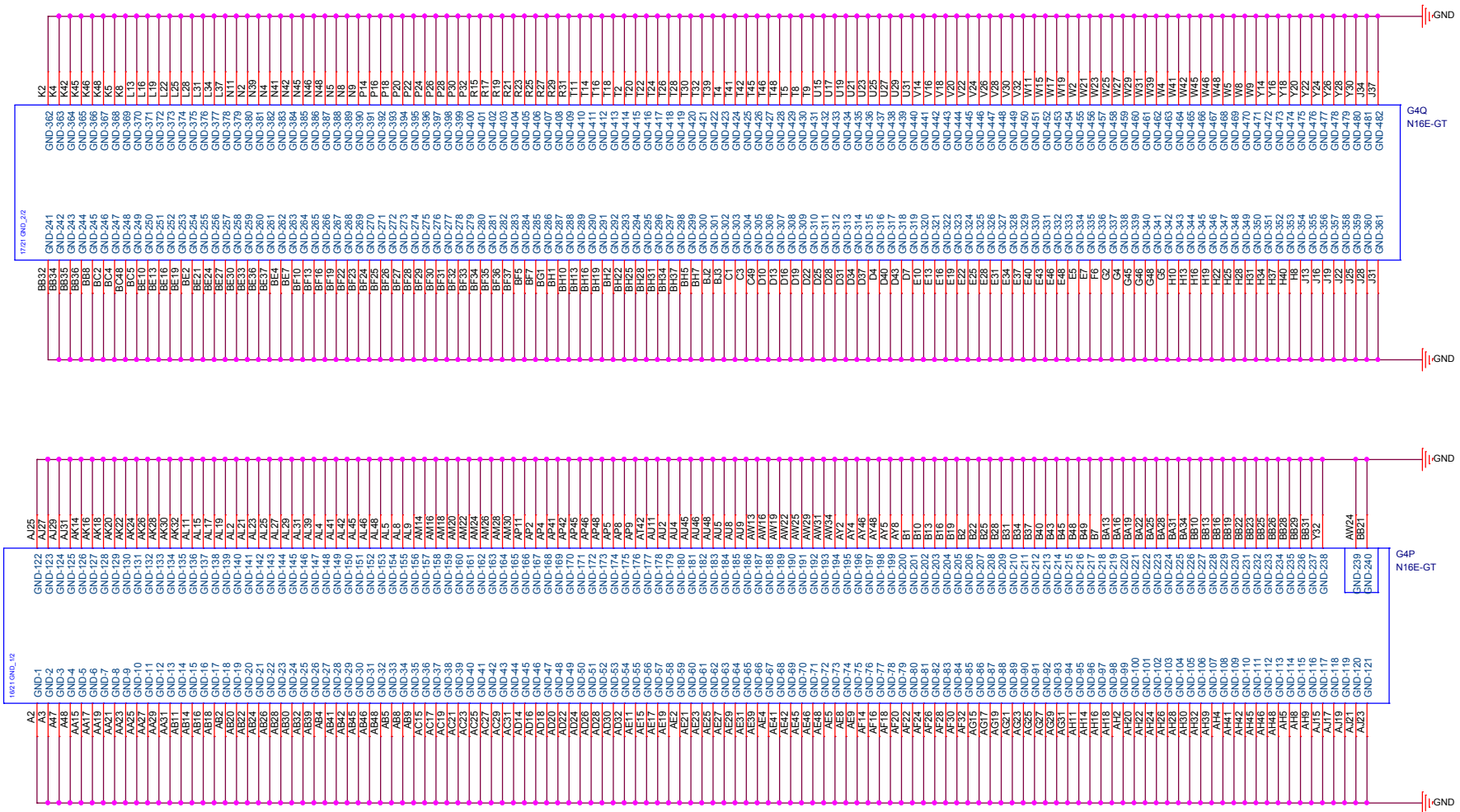


GPU NVVDD, FBVDDQ

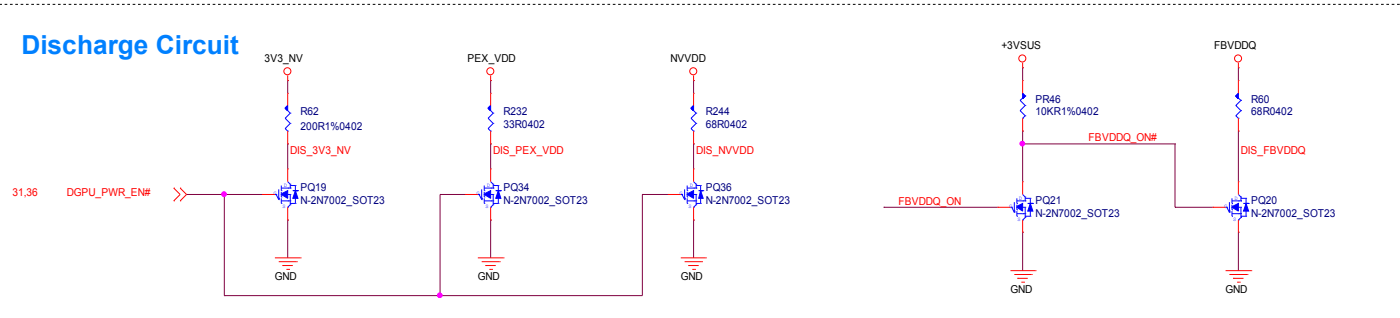
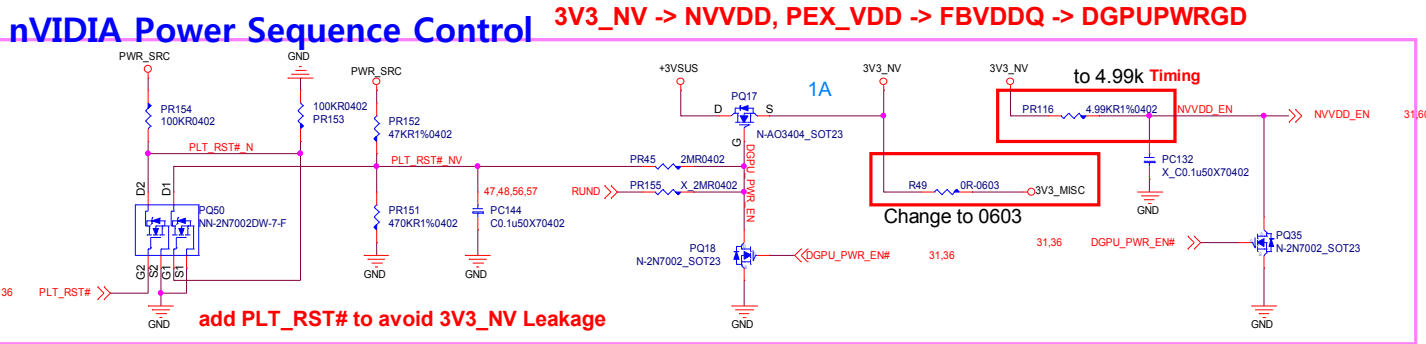
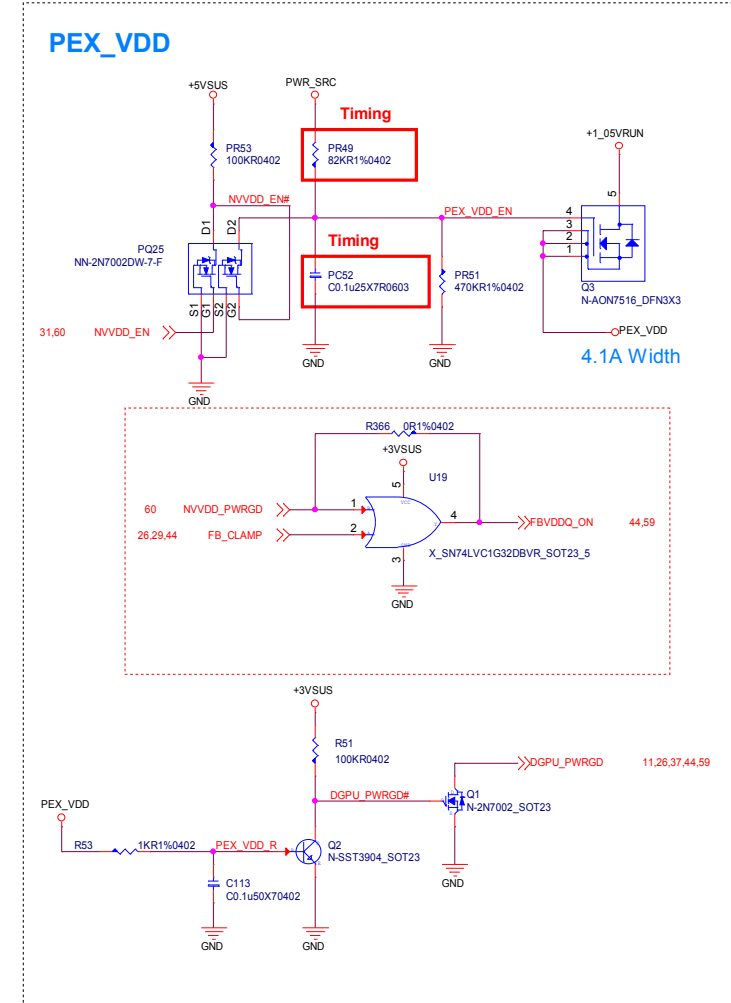
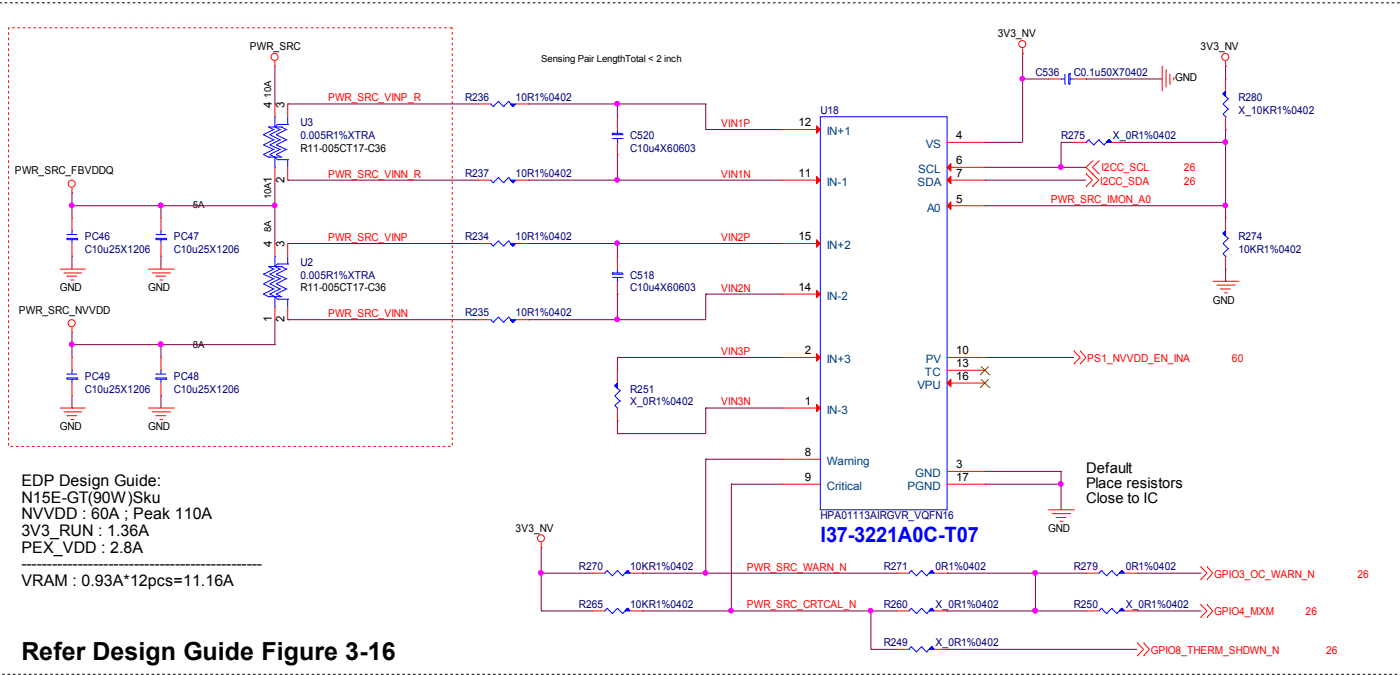




DGPU GND

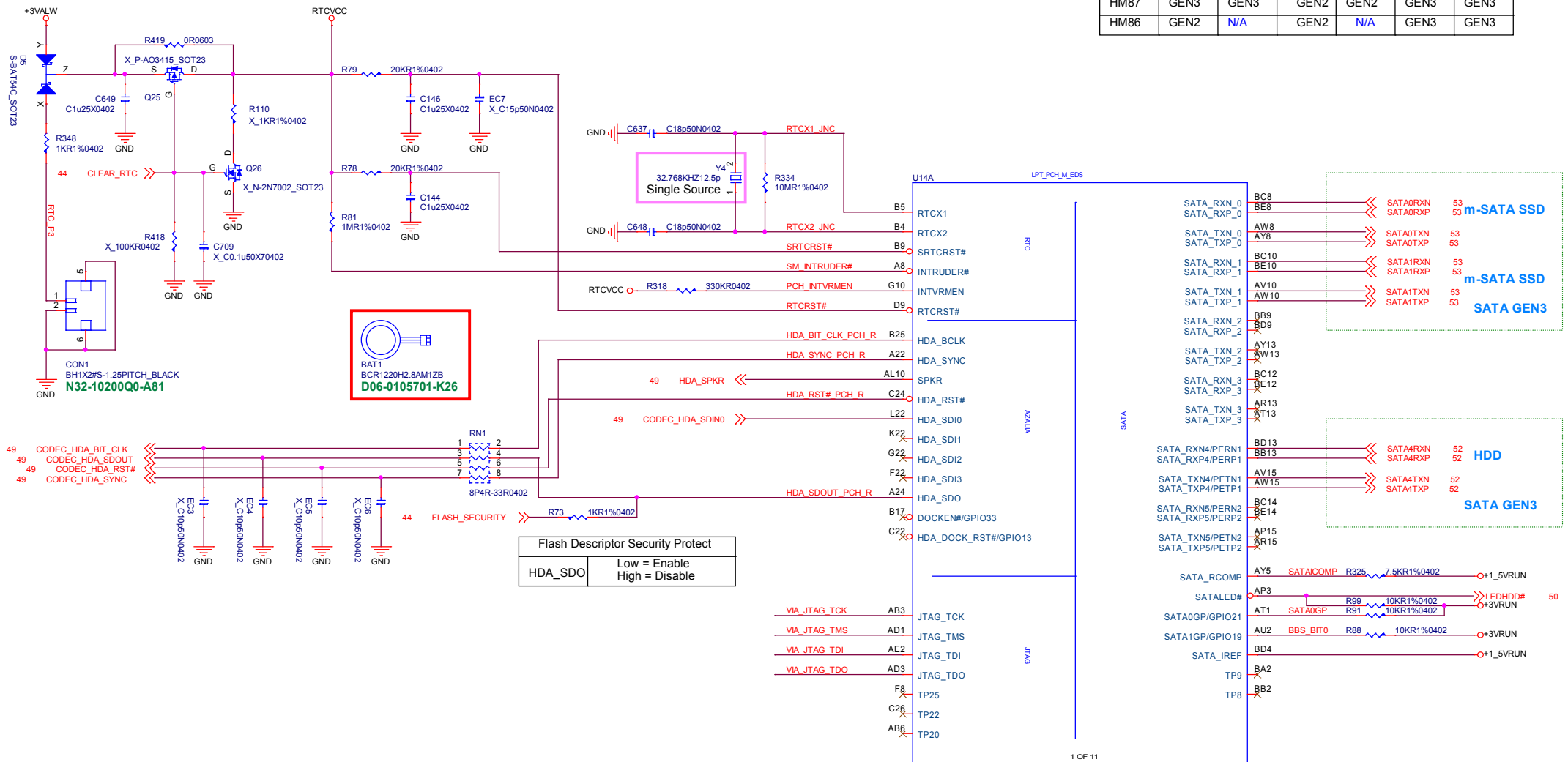


# DGPU\_Power Control



## Lynx Point ( HDA/JTAG/SATA )

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3

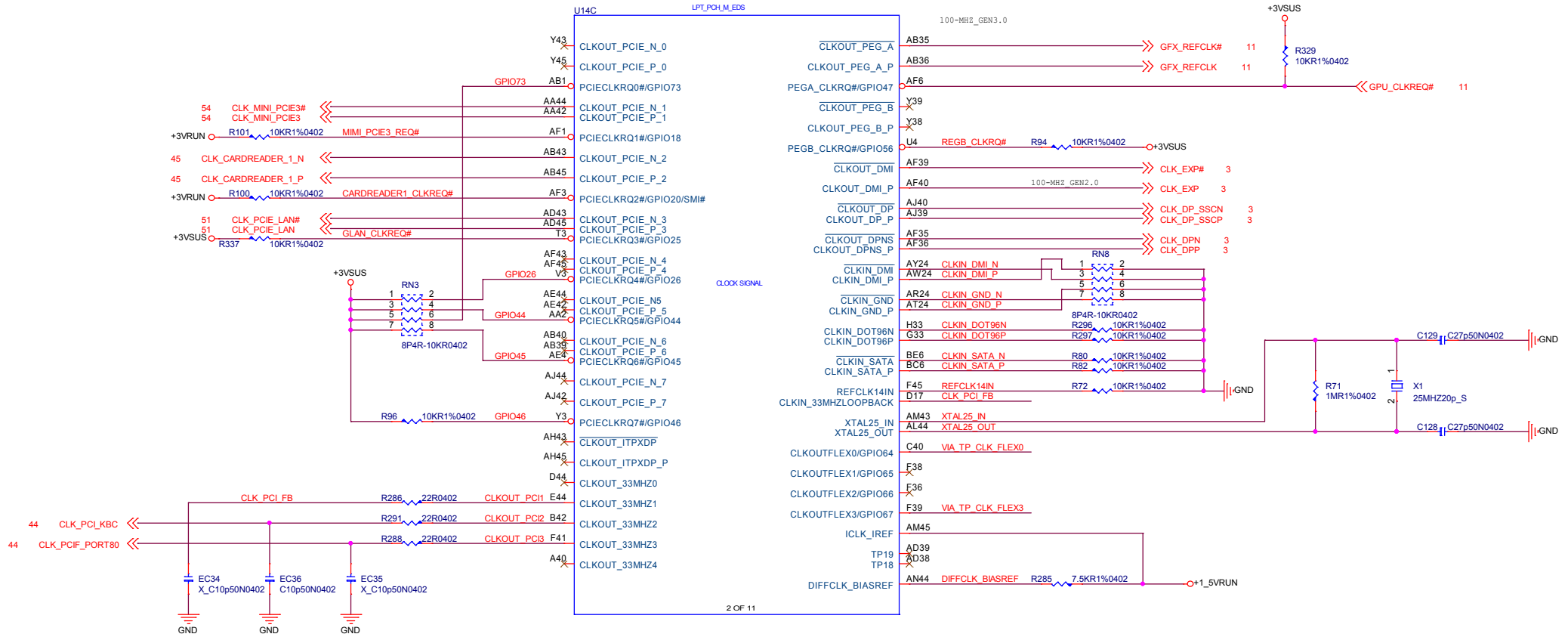


SPK

The Signal has a weak internal pull-down  
 Note: the internal pull-down is disabled after PLTRST# deasserts.  
 If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode  
 (Panther Point will disable the TCO Timer system reboot feature)

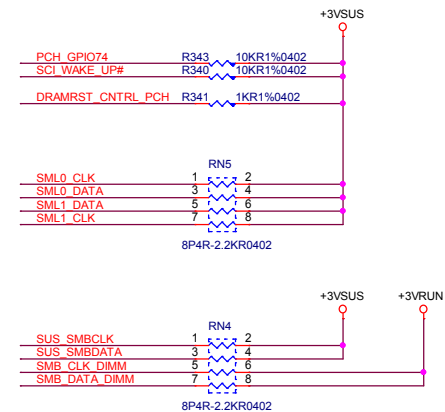
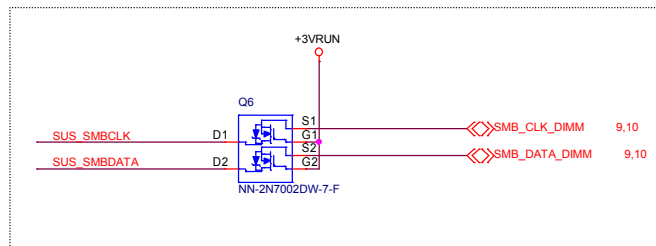
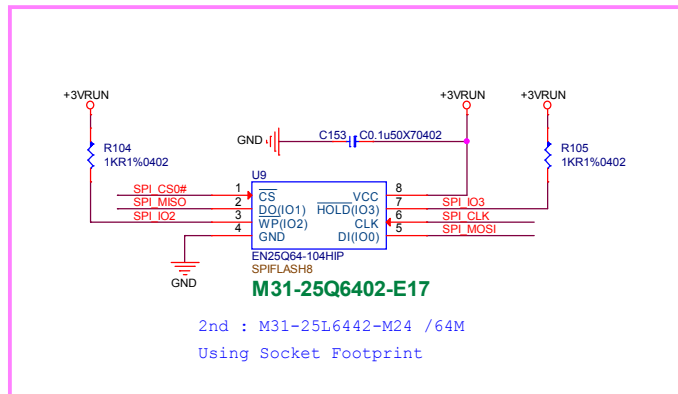
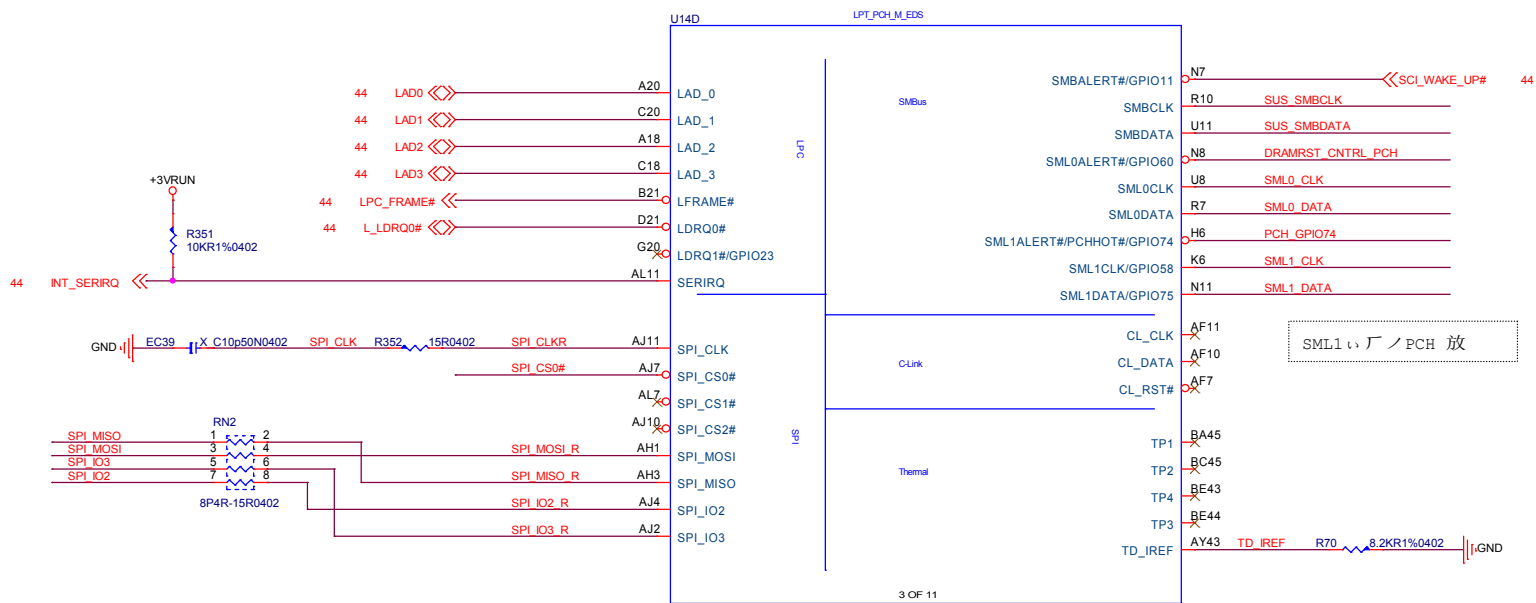
## Lynx Point ( Clock )

PCIE devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.  
Intel recommends terminating PCIECLKREQ# pin on PCH with 10 k  $\pm$  10% external pull-up resistor instead of No Connect.  
Only PCIECLKREQ[2:1]# on PCH are core well powered. All other PCIECLKREQ# are suspend well powered.

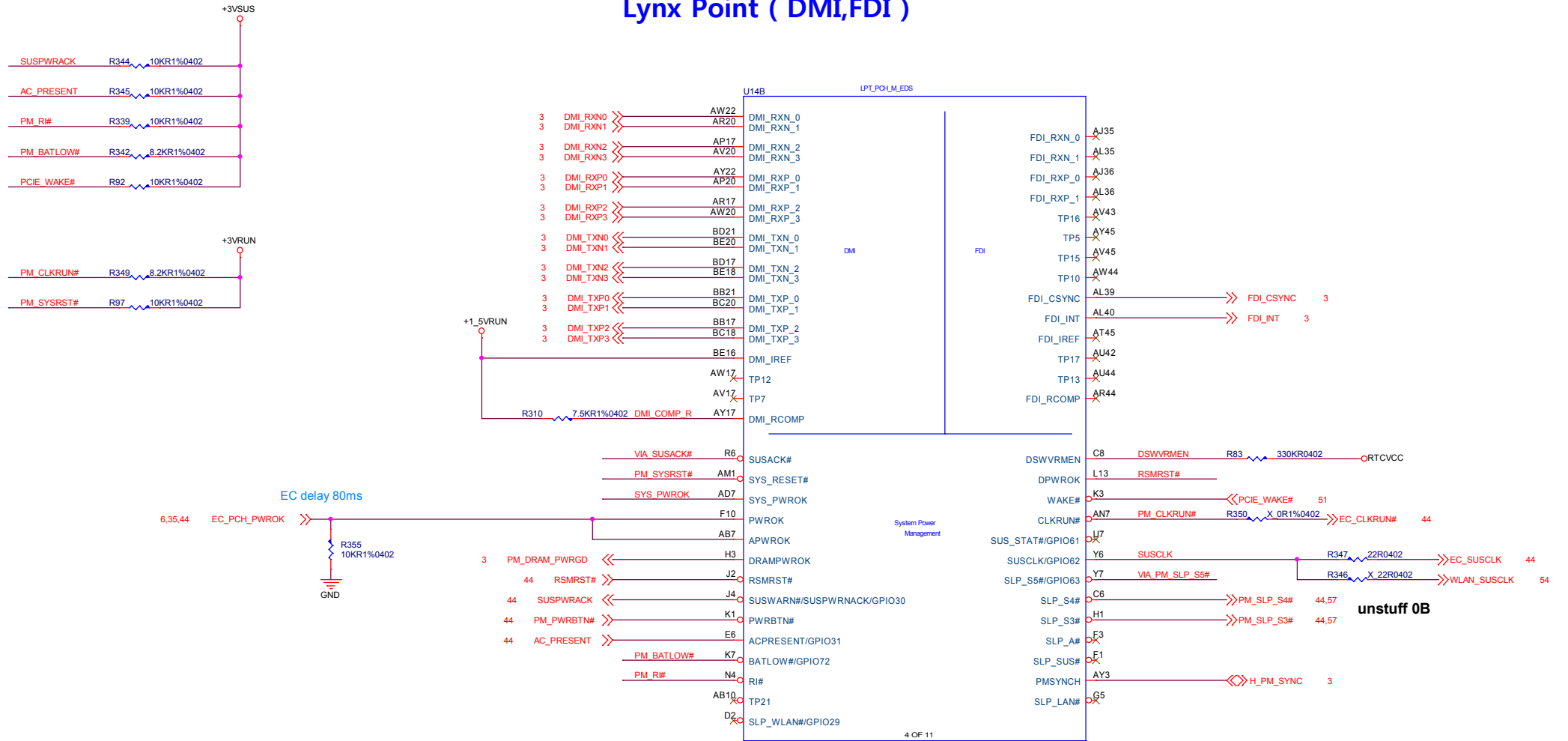


The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

## Lynx Point ( LPC,SMBUS )



# Lynx Point ( DMI,FDI )

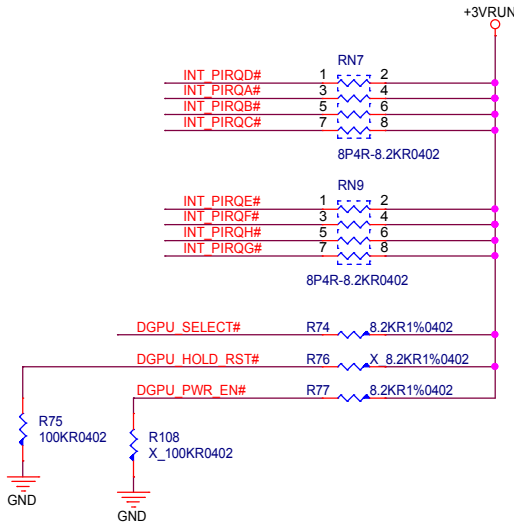


GPIO Setting : Ref 486708\_LPT\_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSXVRMEN - On Die DSX VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

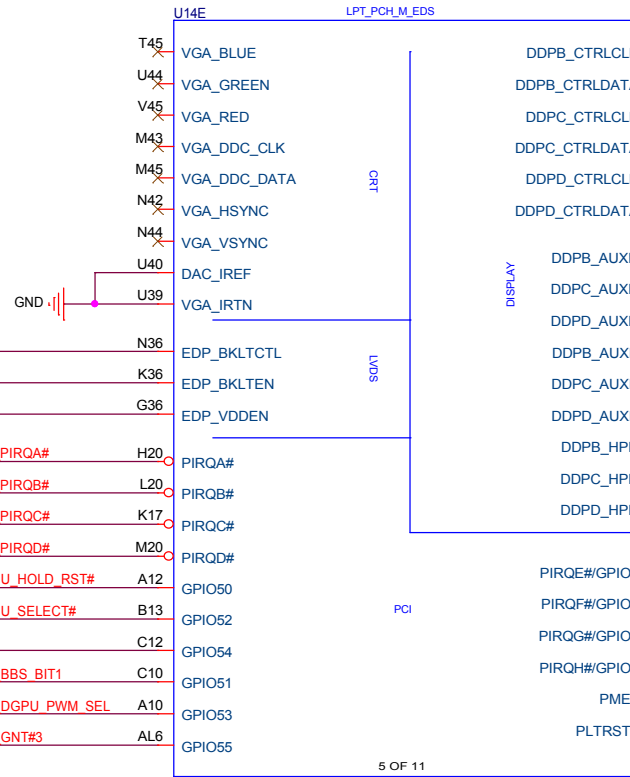
# Lynx Point ( PCI,DDI )



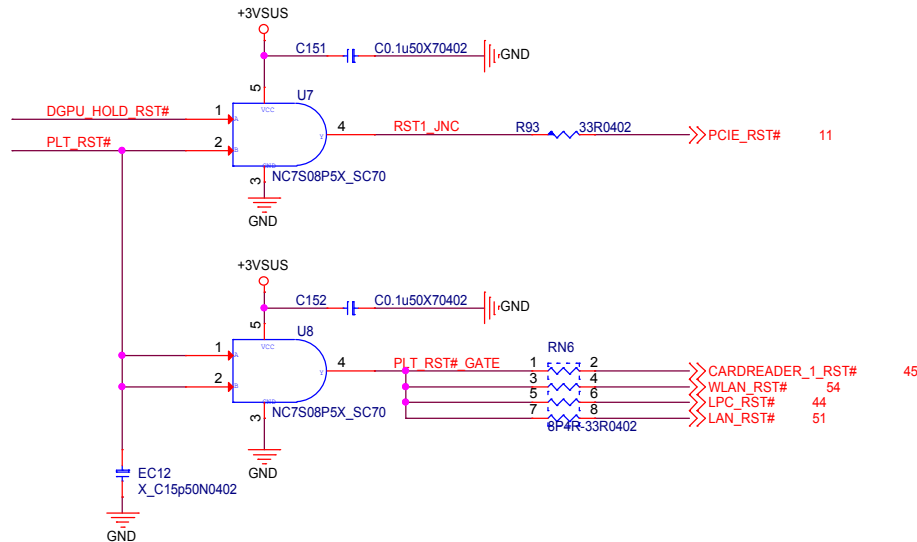
42 EDP\_BKLTCTL <<< N36  
42 EDP\_BKLTEN <<< K36  
42 EDP\_VDDEN <<< G36

31 DGPU\_PWR\_EN# <<< C12

INT\_PIRQA# H20 PIRQA#  
INT\_PIRQB# L20 PIRQB#  
INT\_PIRQC# K17 PIRQC#  
INT\_PIRQD# M20 PIRQD#  
DGPU\_HOLD\_RST# A12 GPIO50  
DGPU\_SELECT# B13 GPIO52  
VIA BBS\_BIT1 C10 GPIO54  
VIA DGPU\_PWM\_SEL A10 GPIO51  
VIA GNT#3 AL6 GPIO53  
GPIO55



DDI-B : DP  
DDI-C : HDMI



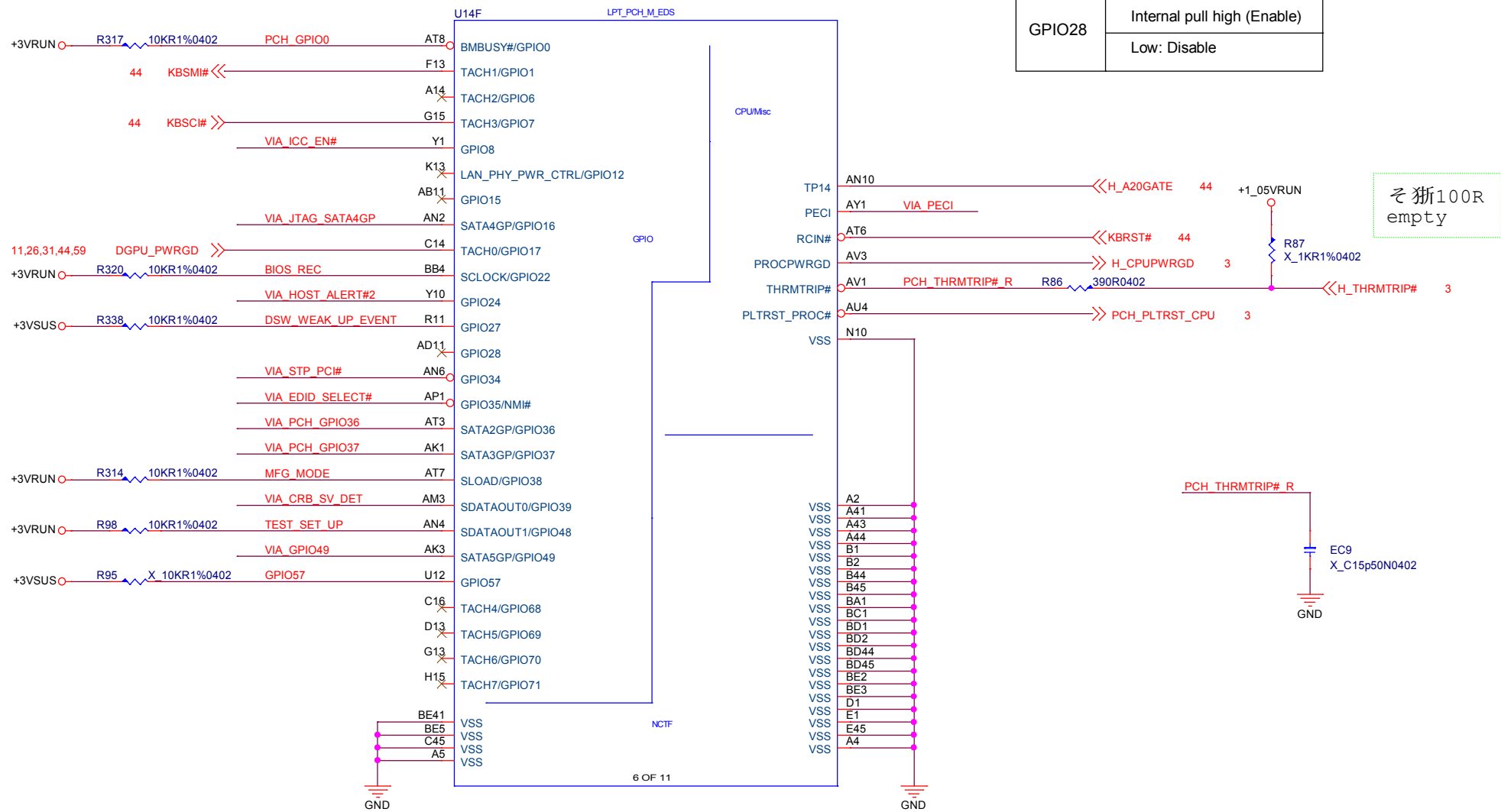
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI



# Lynx Point ( GPIO,MISC )

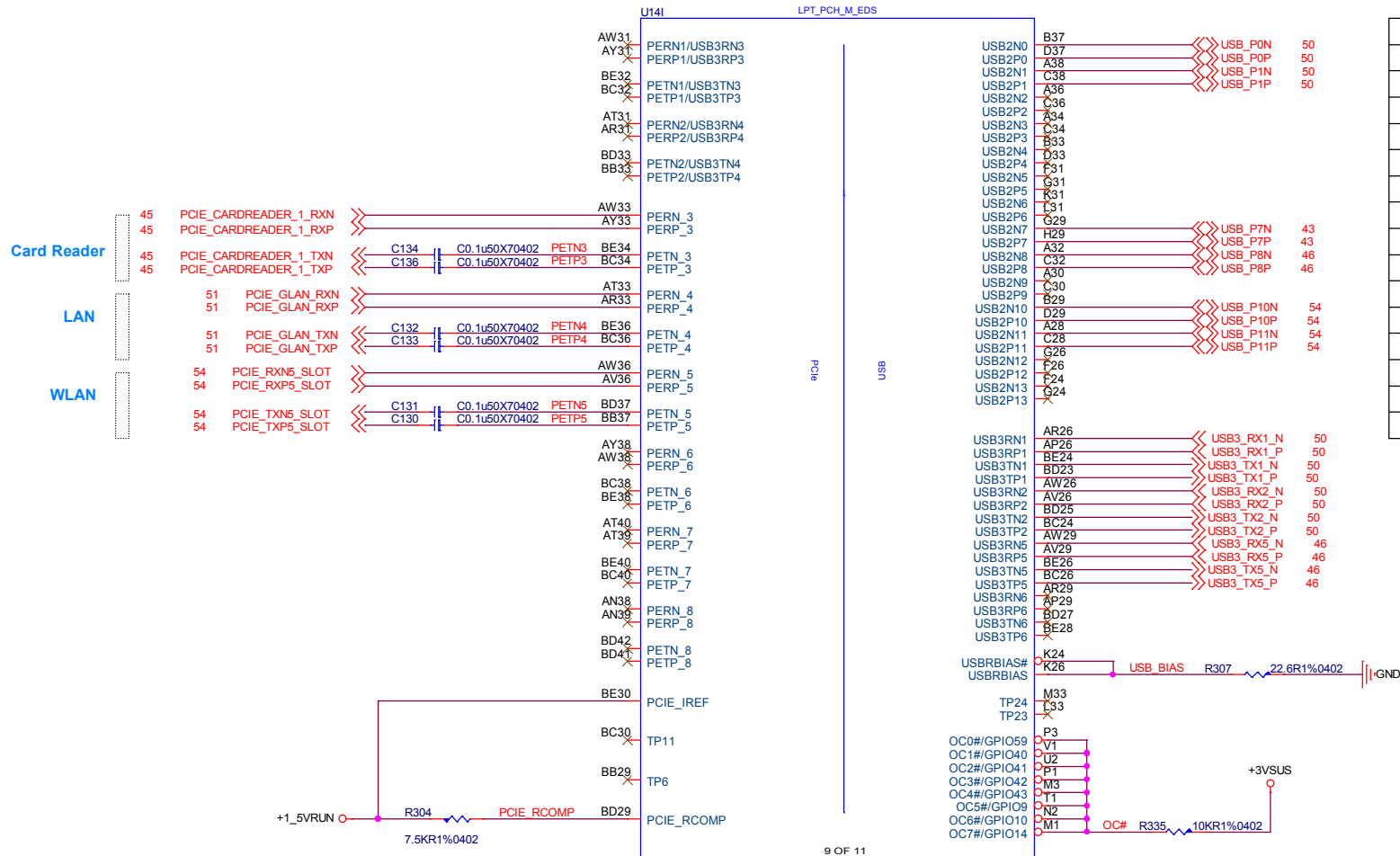
GPIO Setting : Ref 486708\_LPT\_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



# Lynx Point ( PCIE,USB )

Intel Lynx Point ECHI USB(2.0) debug transport 惠铂Port1 or Port9



USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16H5A
1	2	USB 3.0 Port 2	16H5A
2			
3			NC
4			NC
5			NC
6			NC
7		EPF021	
8	3	USB 3.0 Port 5	16H51
9			
10		WLAN	
11		WebCam	
12			NC
13			NC

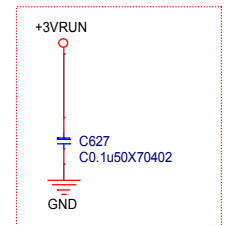
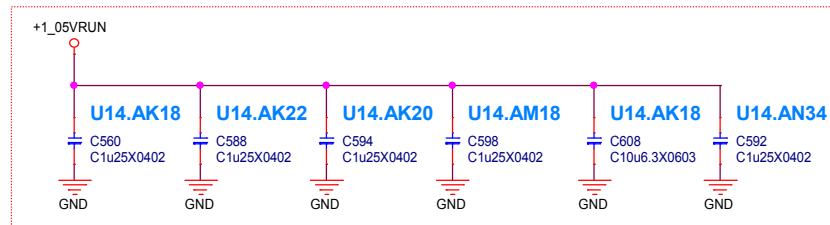
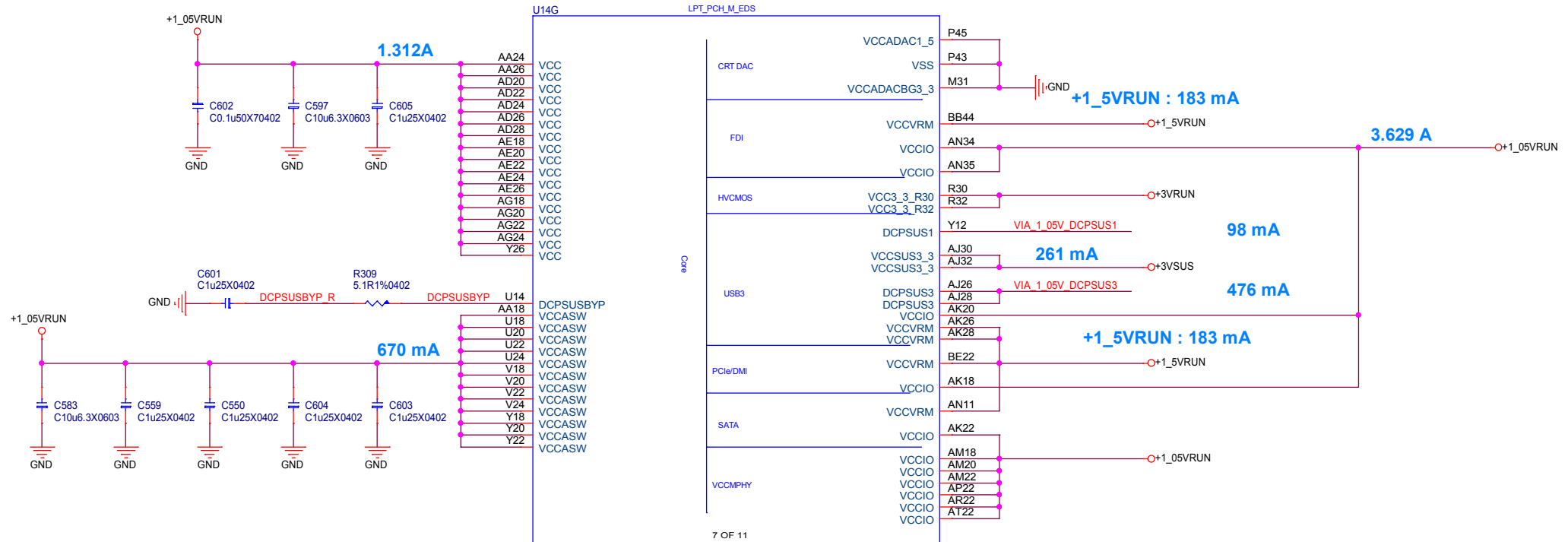
HM86 USB3.0 PORT 5,6



MICRO-STAR INT'L CO.,LTD.

Title <b>PCH-7 ( PCIE,USB )</b>		
Size	Document Number <b>MS-16H5</b>	Rev <b>1.1</b>
Date:	Tuesday, July 15, 2014	Sheet 38 of 72

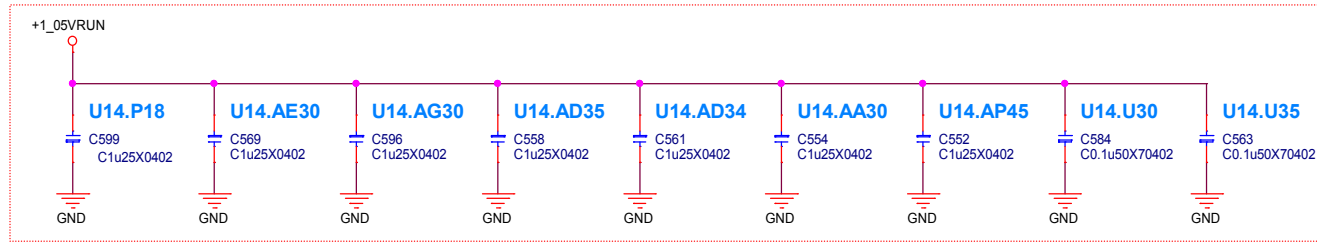
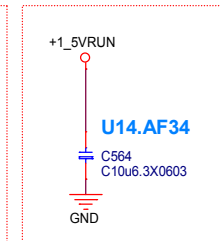
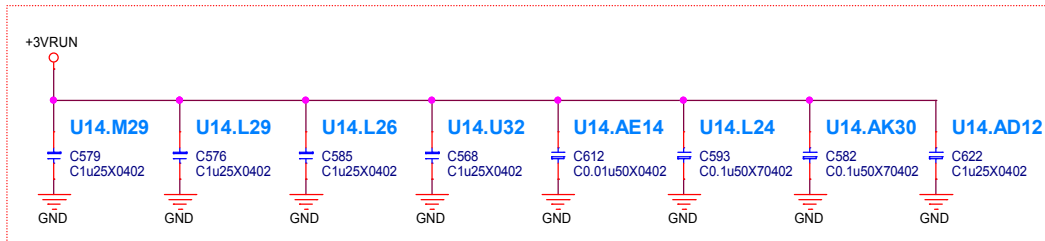
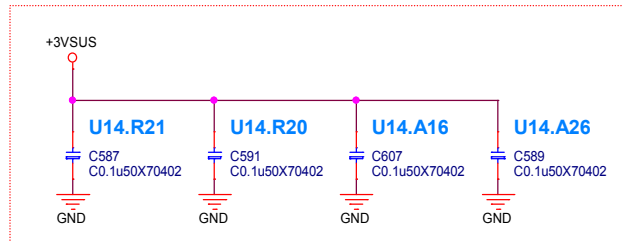
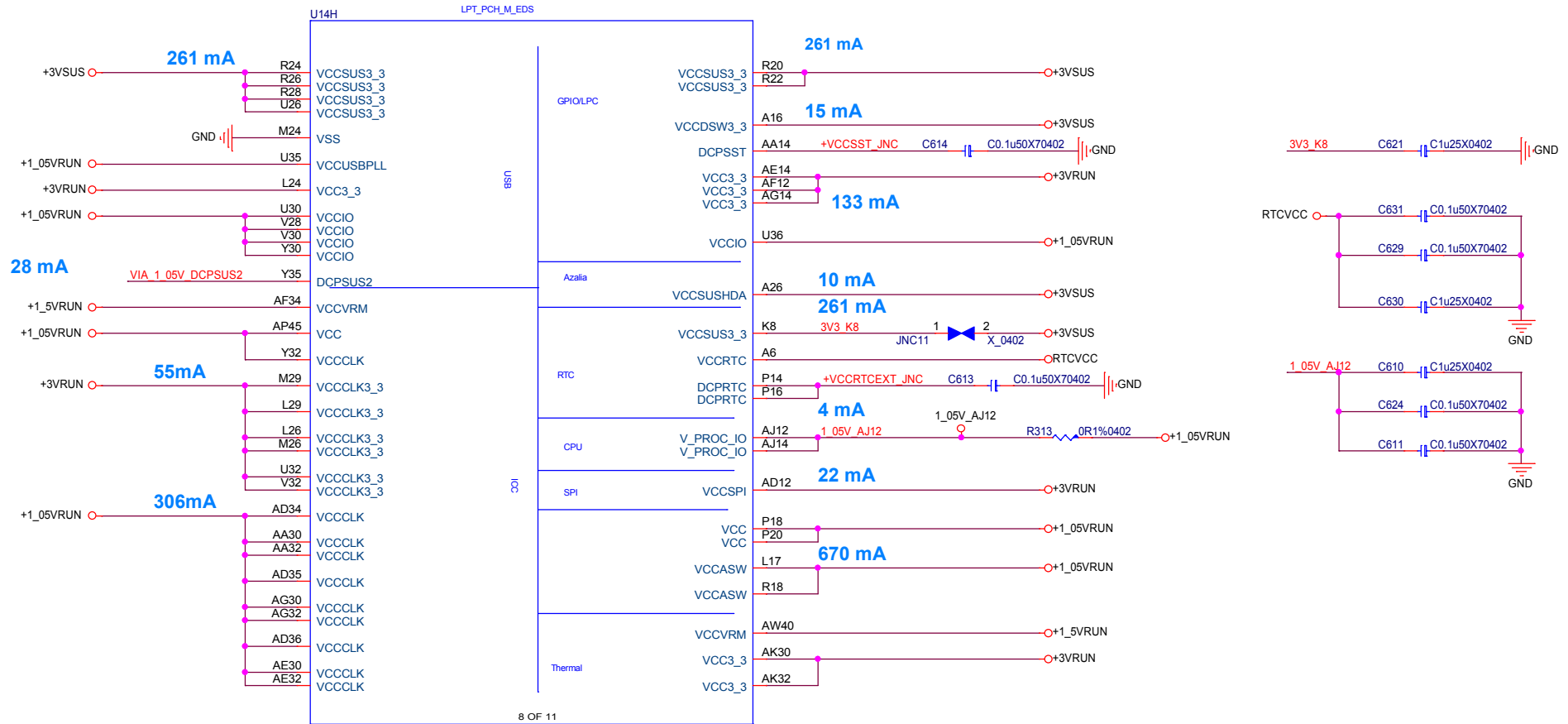
# Lynx Point ( Power )



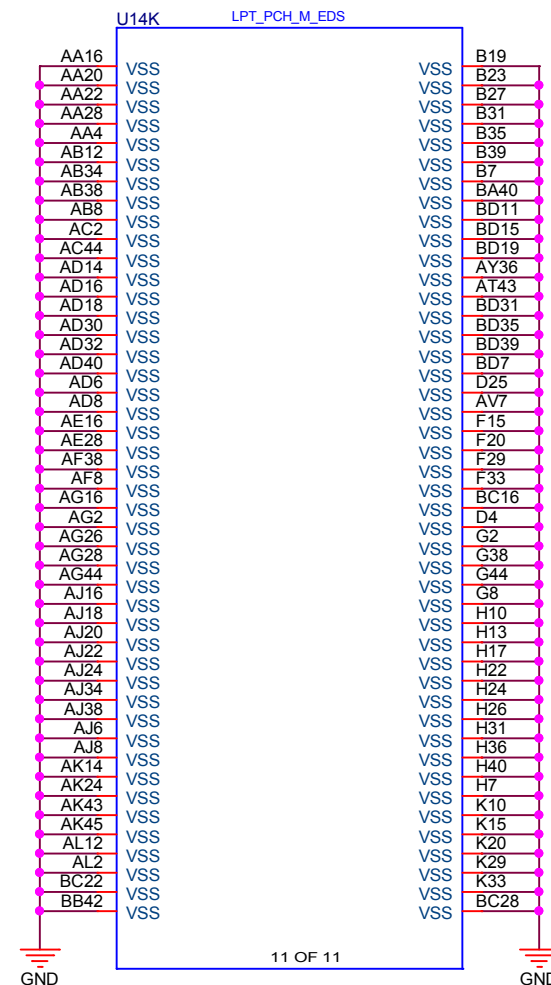
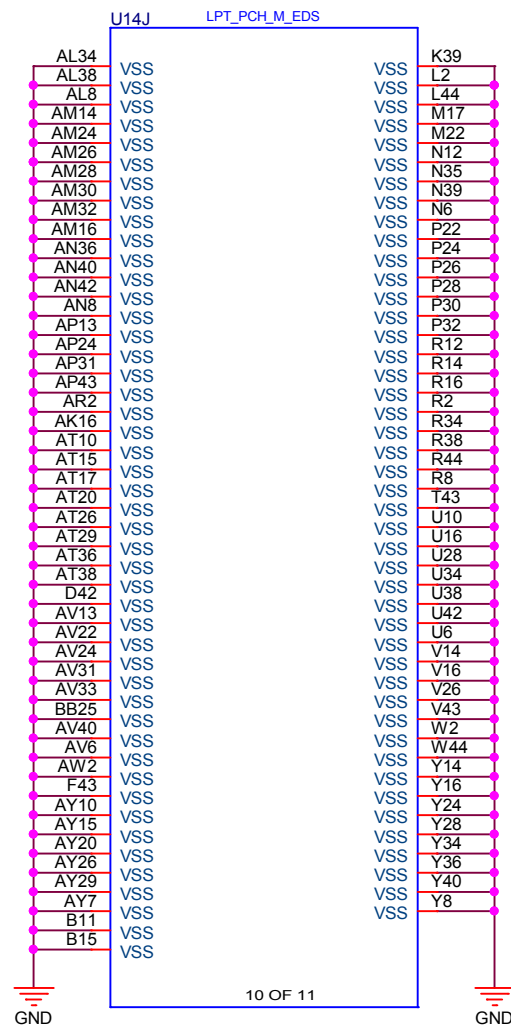
MICRO-STAR INT'L CO.,LTD.

Title		
PCH-8 ( Power )		
Size	Document Number	Rev
	MS-16H5	1.1
Date:	Tuesday, July 15, 2014	Sheet 39 of 72

# Lynx Point ( Power )



# Lynx Point ( GND )

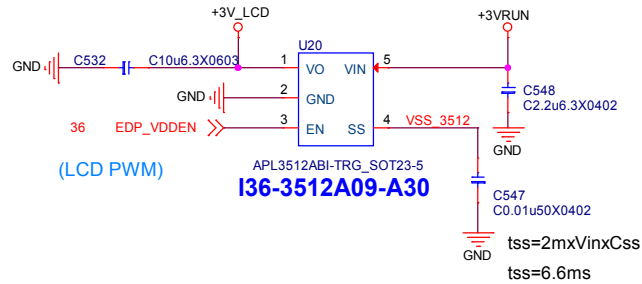


MICRO-STAR INT'L CO.,LTD.

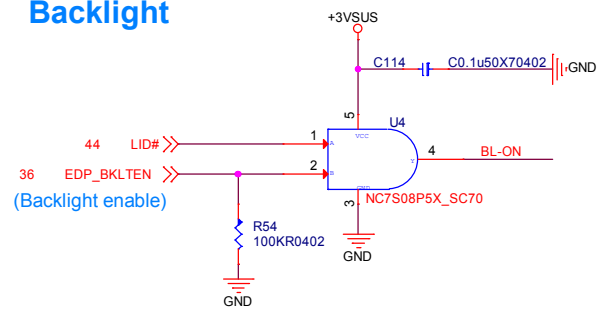
Title		
PCH-8 ( GND )		
Size	Document Number	Rev
	MS-16H5	1.1
Date:	Tuesday, July 15, 2014	Sheet 41 of 72

# eDP Connector

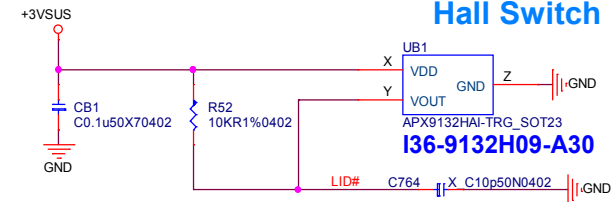
## Pannel Device Logic Power



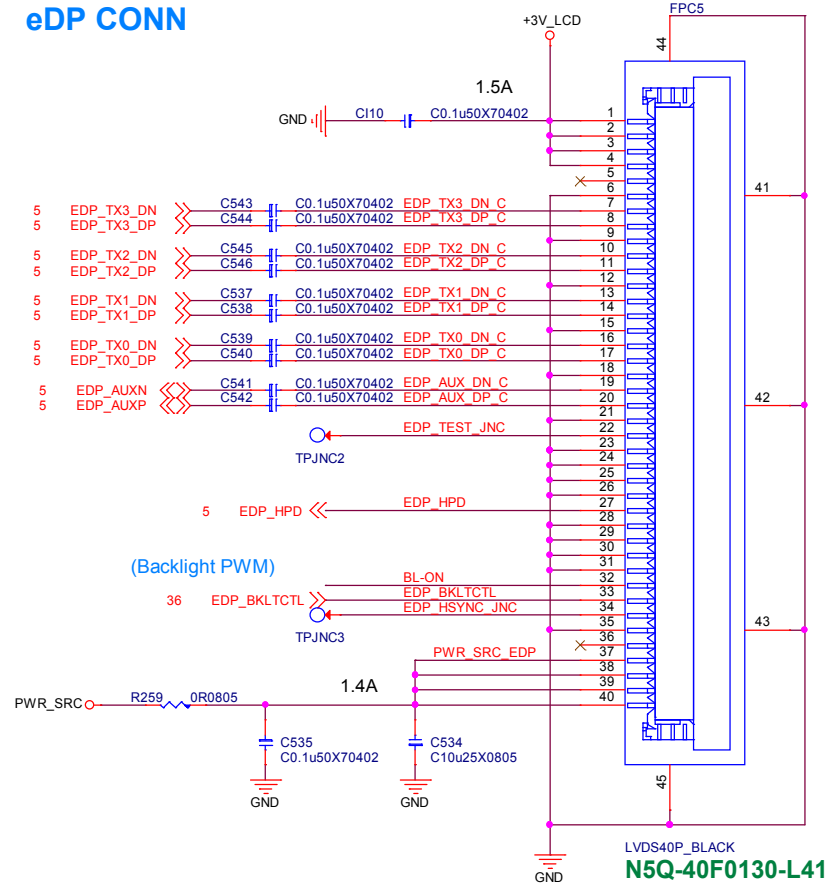
## Backlight



## Hall Switch



## eDP CONN

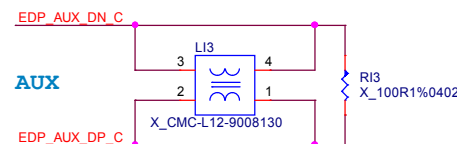
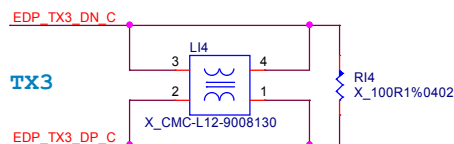
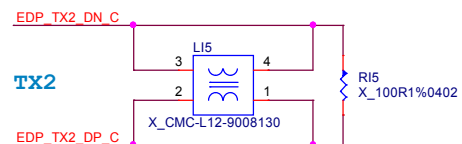
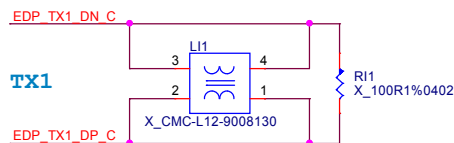
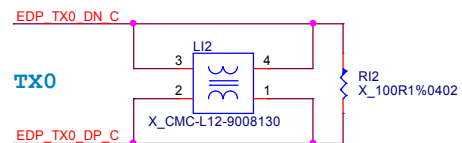


## LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDP	HPDP signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

Place Close eDP Connector

Reserve for EMI

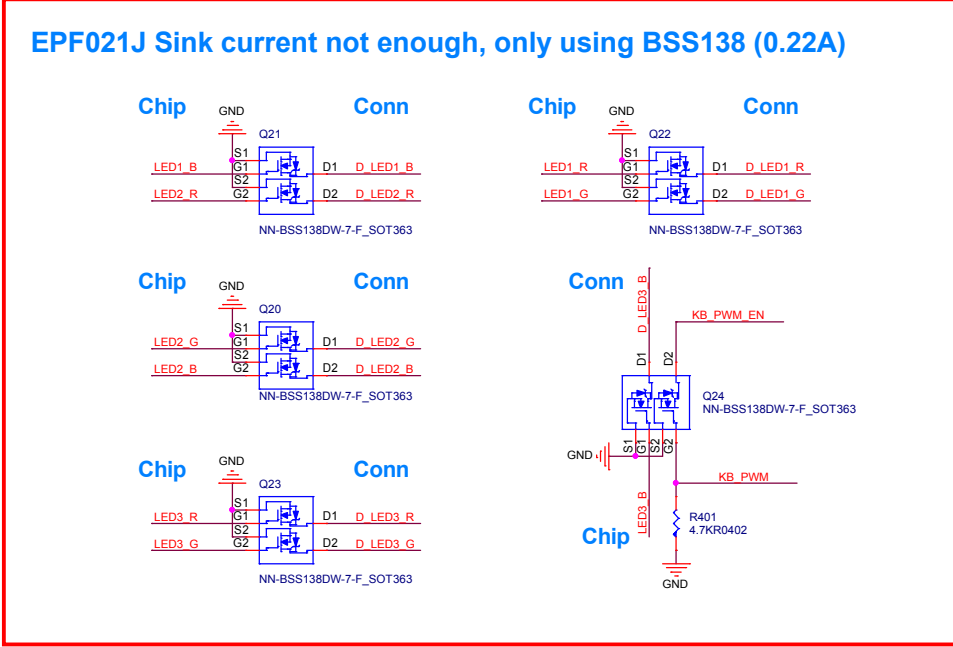
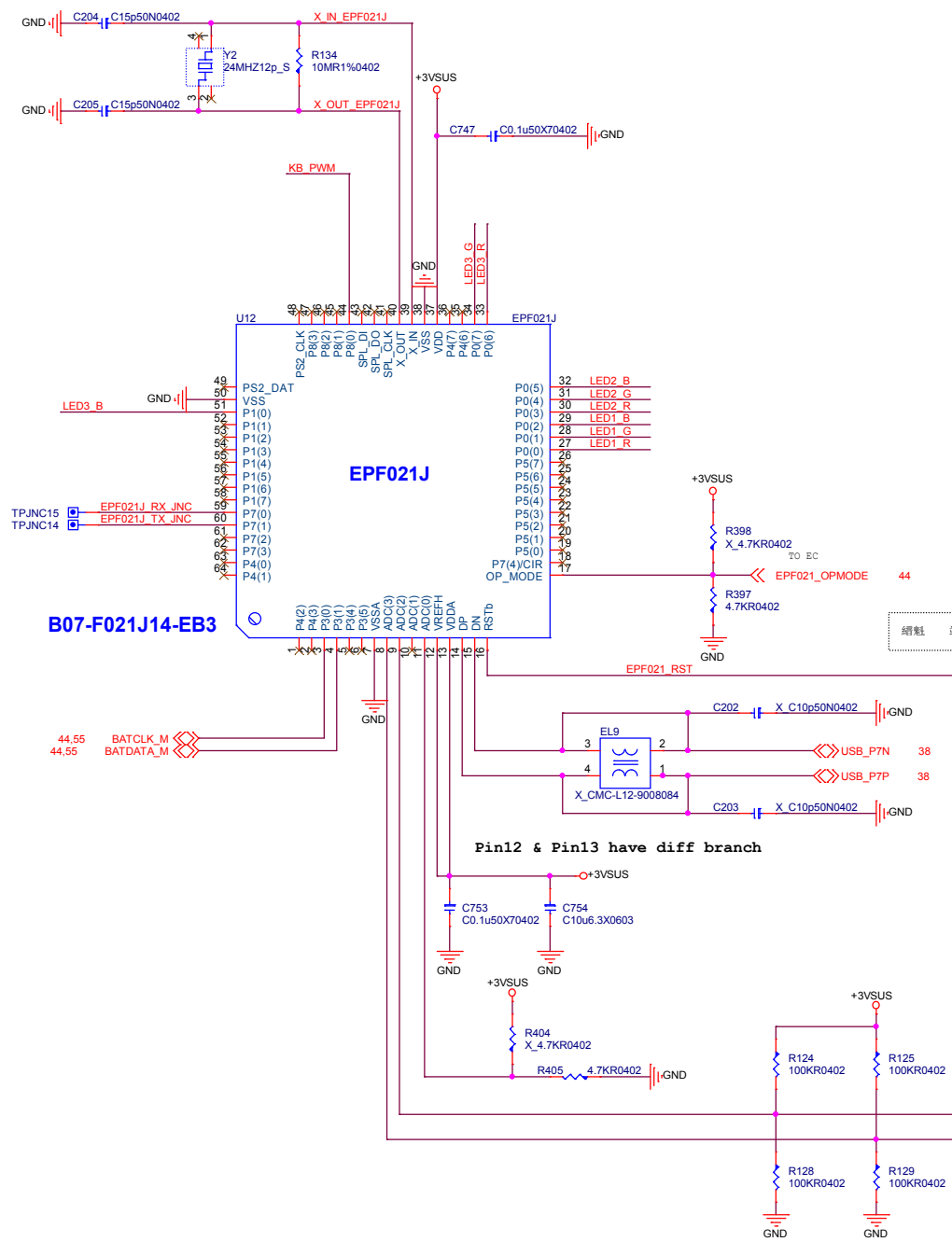


msi

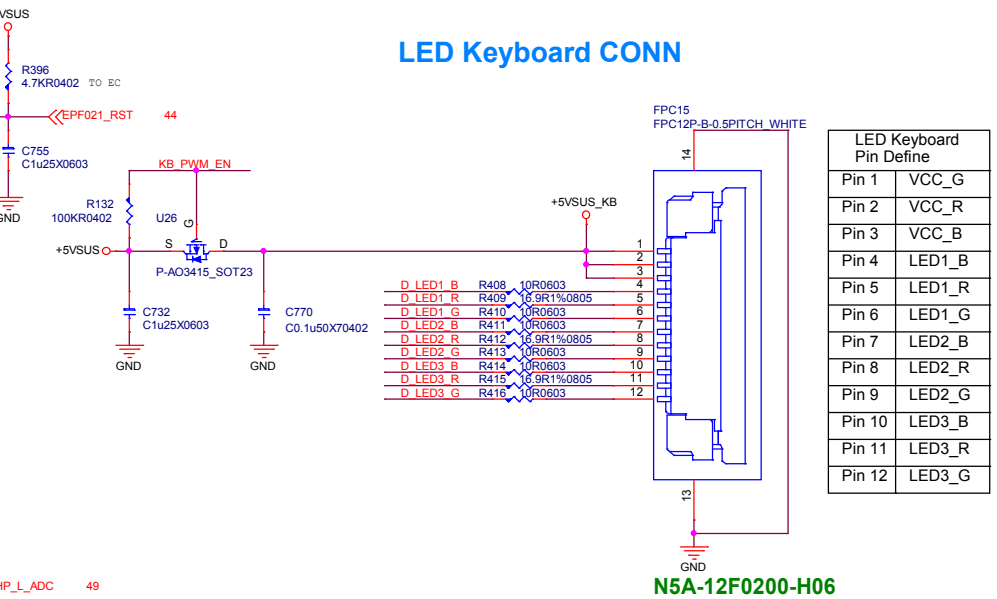
MICRO-STAR INT'L CO.,LTD.

Title <b>eDP Connector</b>		
Size	Document Number <b>MS-16H5</b>	Rev <b>1.1</b>
Date:	Tuesday, July 15, 2014	Sheet 42 of 72

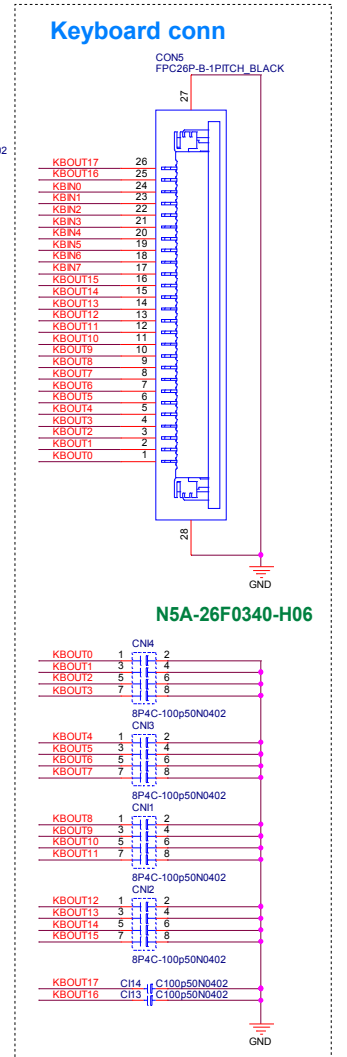
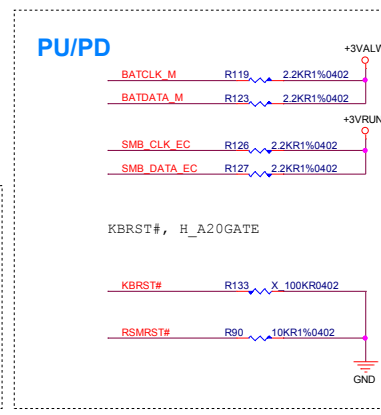
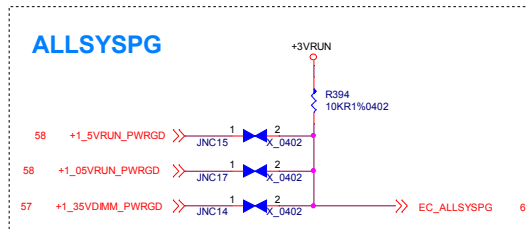
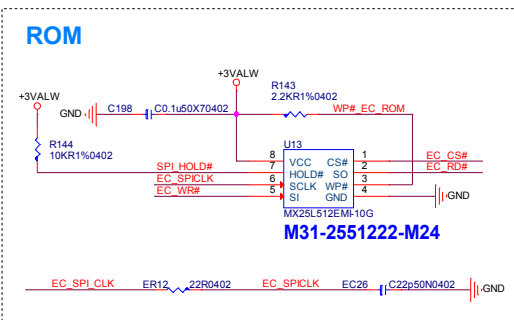
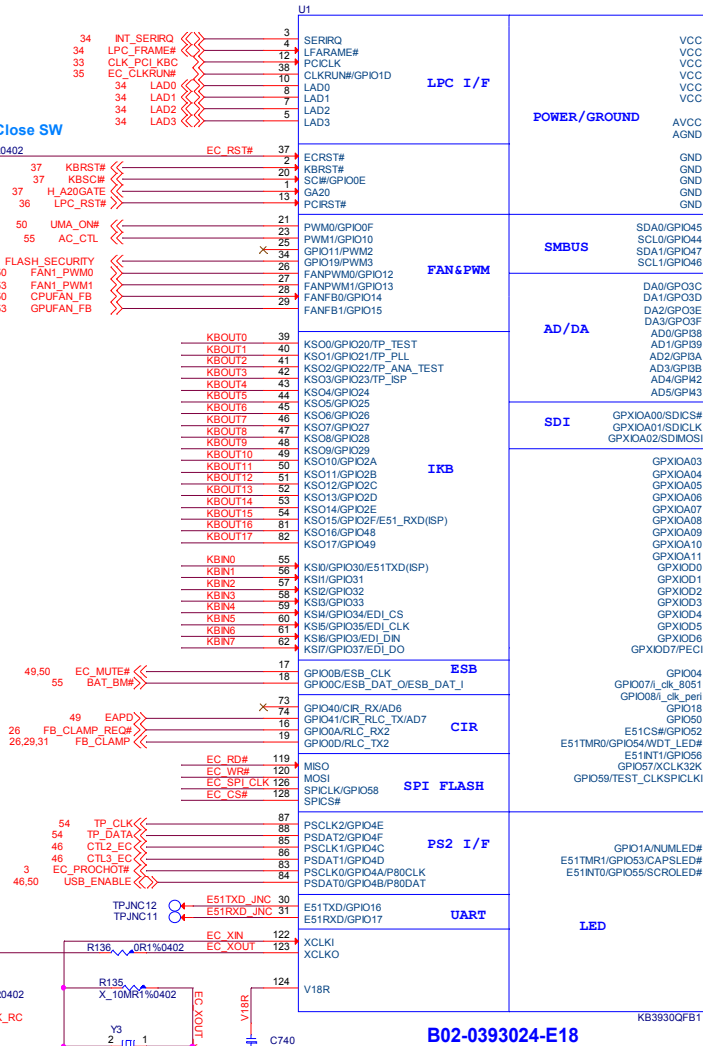
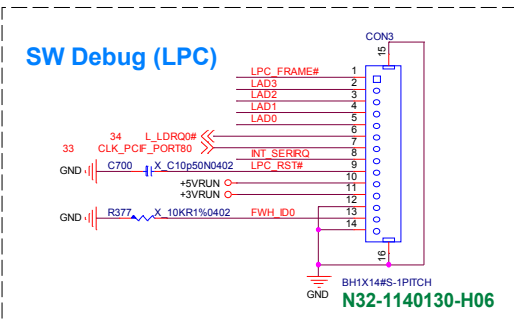
# LED 8051 Controller



## LED Keyboard CONN





[illegible]

# CardReader ( RTS5249 )

RTS5249 Colay RTS5227

Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227

## Power Trace

Pin11(3V3\_IN) / Pin 12(CARD\_3V3)trace fixed width is 40 mils (minimum)

Pin27(3V3aux) / Pin 13(SD\_VDD2)trace fixed width is 30 mils (minimum)

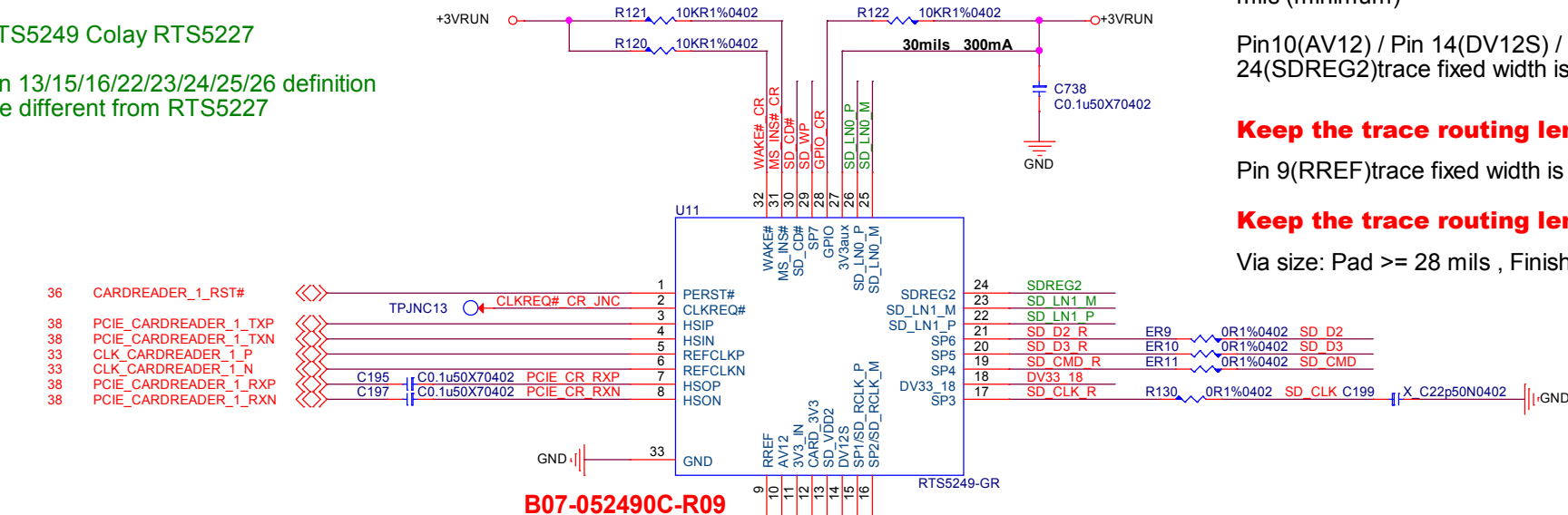
Pin10(AV12) / Pin 14(DV12S) / Pin 18(DV33\_18) / Pin 24(SDREG2)trace fixed width is 20 mils (minimum)

Keep the trace routing lengths is limit to 200 mils

Pin 9(RREF)trace fixed width is 12 mils (minimum)

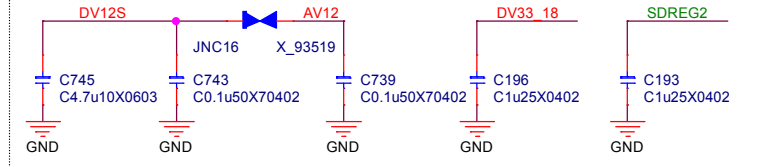
Keep the trace routing lengths is limit to 200 mils

Via size: Pad >= 28 mils , Finished hole >= 16 mils.

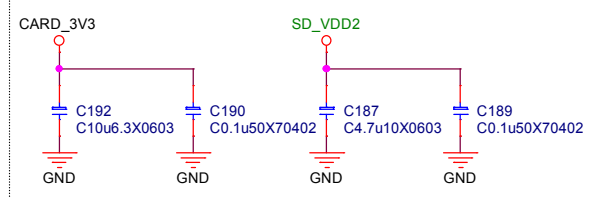


B07-052490C-R09

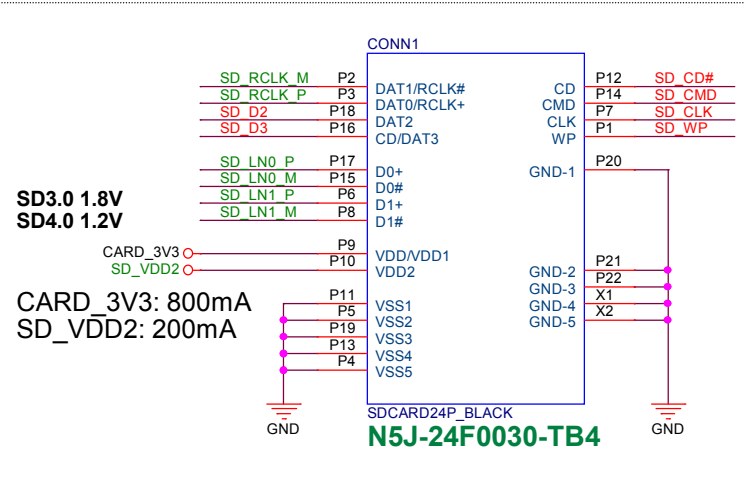
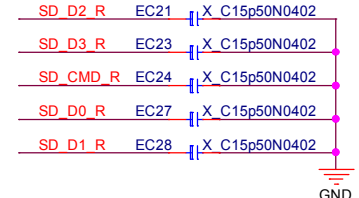
## Close Chip



## Close Connector



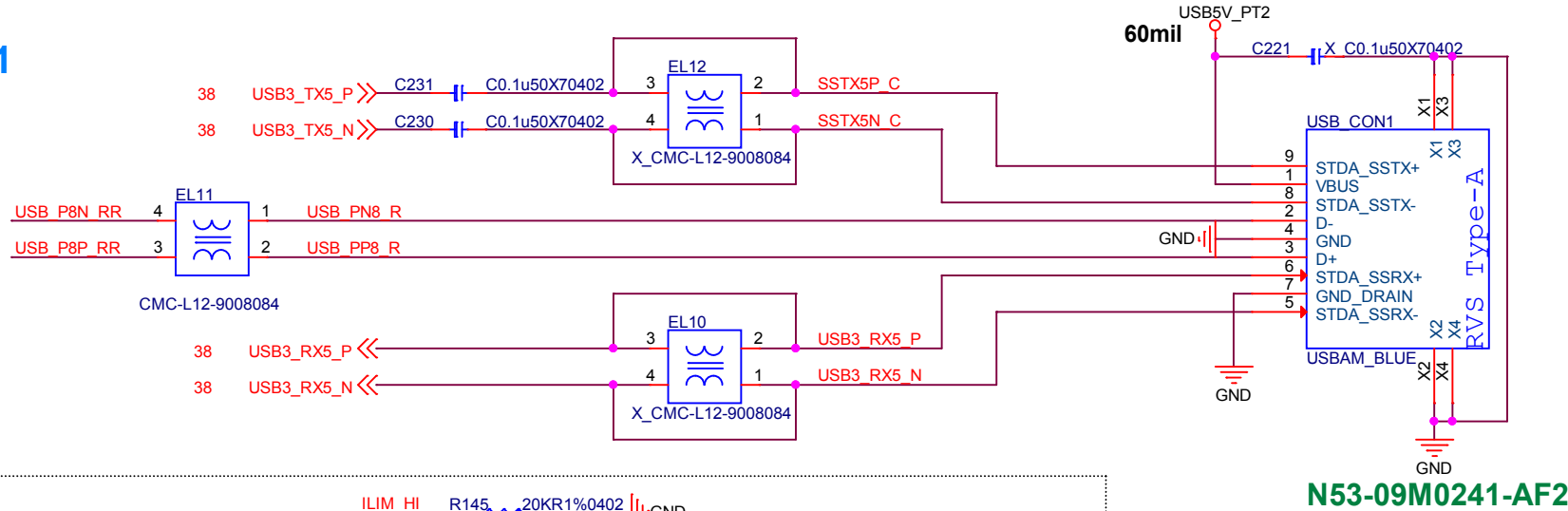
## EMI



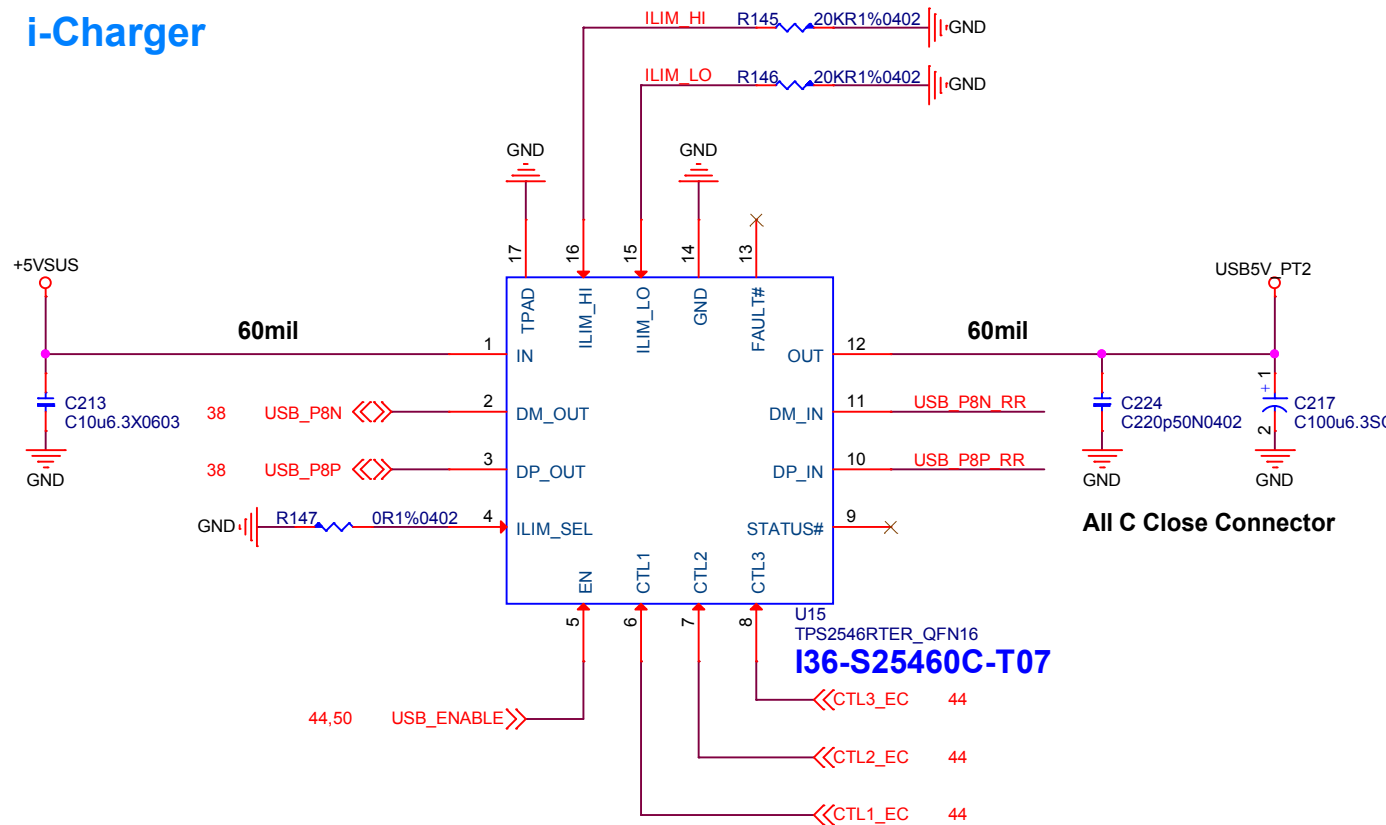
# USB 3.0 / iCharger

## USB3.0 CNT-1

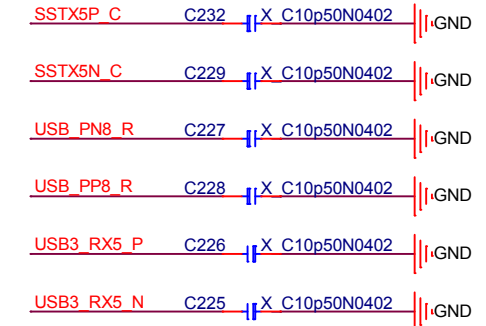
USB3.0 Port-6  
USB2.0 Port-8



## i-Charger



## EMI

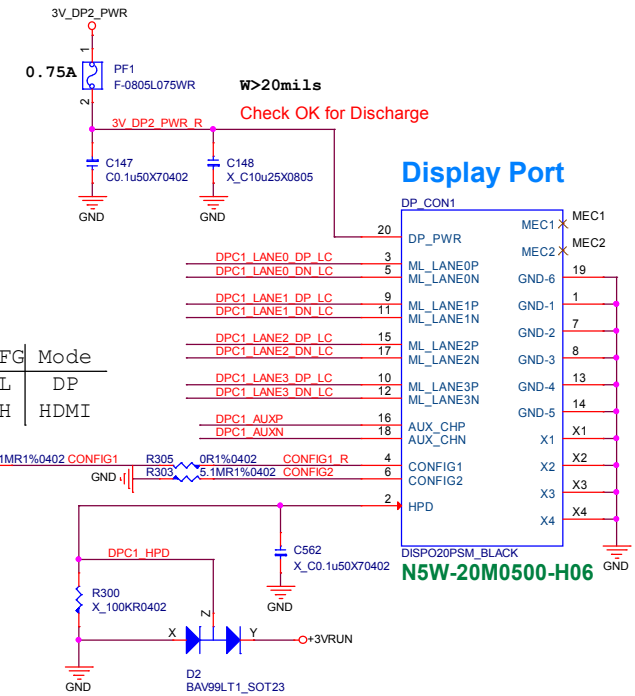
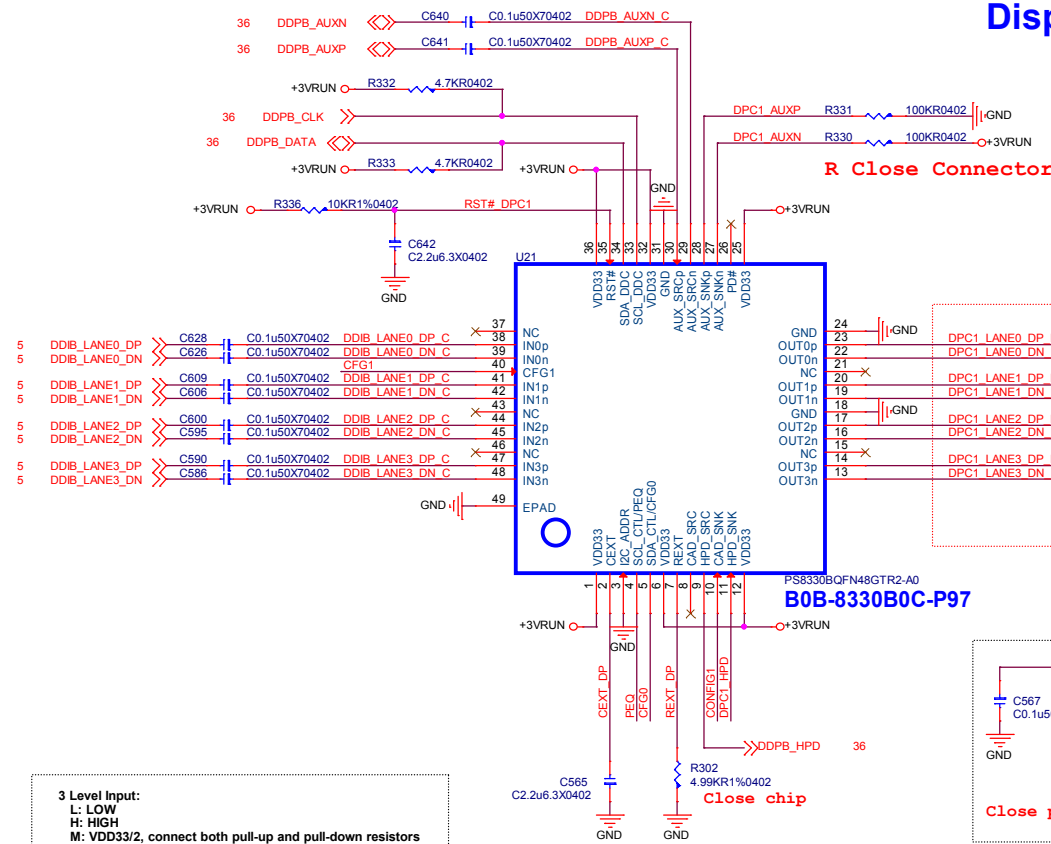


msi

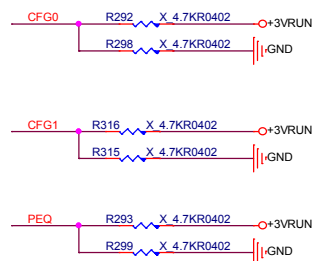
MICRO-STAR INT'L CO.,LTD.

Title					<b>USB 3.0 / iCharger</b>					
Size		Document Number					Rev		1.1	
		<b>MS-16H5</b>								
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## Display Port



CAD\_SNK have internal Pull down 1Mohm.  
HPD\_SNK Have internal Pull down 150kohm.  
No problem with Leakage from DP device  
The DP\_PWR and RETURN pins of the  
box-to-box connectors must support the  
maximum current rating of 500mA.

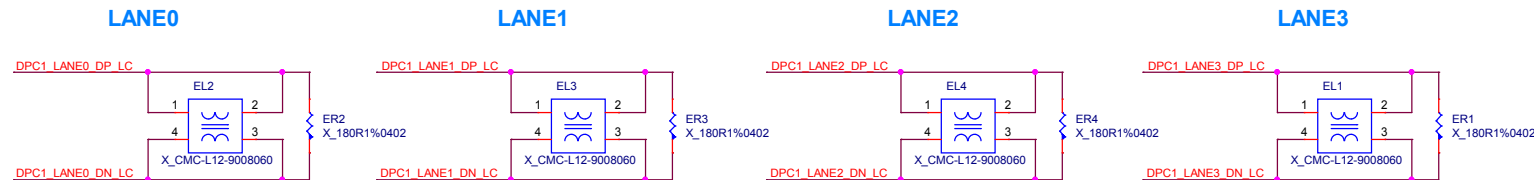


Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.  
 L: default, automatic EQ enable & AUX interception enable  
 M: automatic EQ disable & AUX interception enable  
 H: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

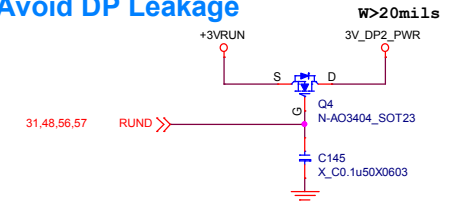
```
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable
```

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.  
 L: default, LEQ, compensate channel loss up to 12dB @ HBR2  
 H: HEQ, compensate channel loss up to 15dB @ HBR2  
 M: LLEQ, compensate channel loss up to 5dB @ HBR2

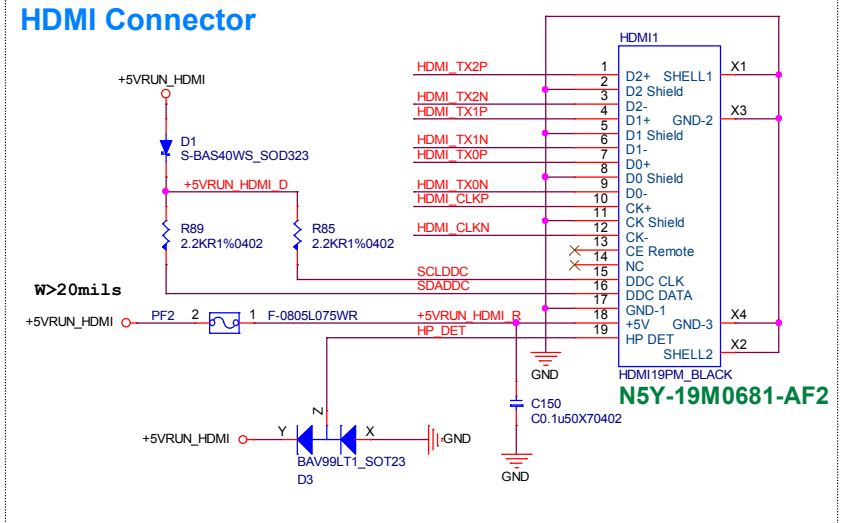
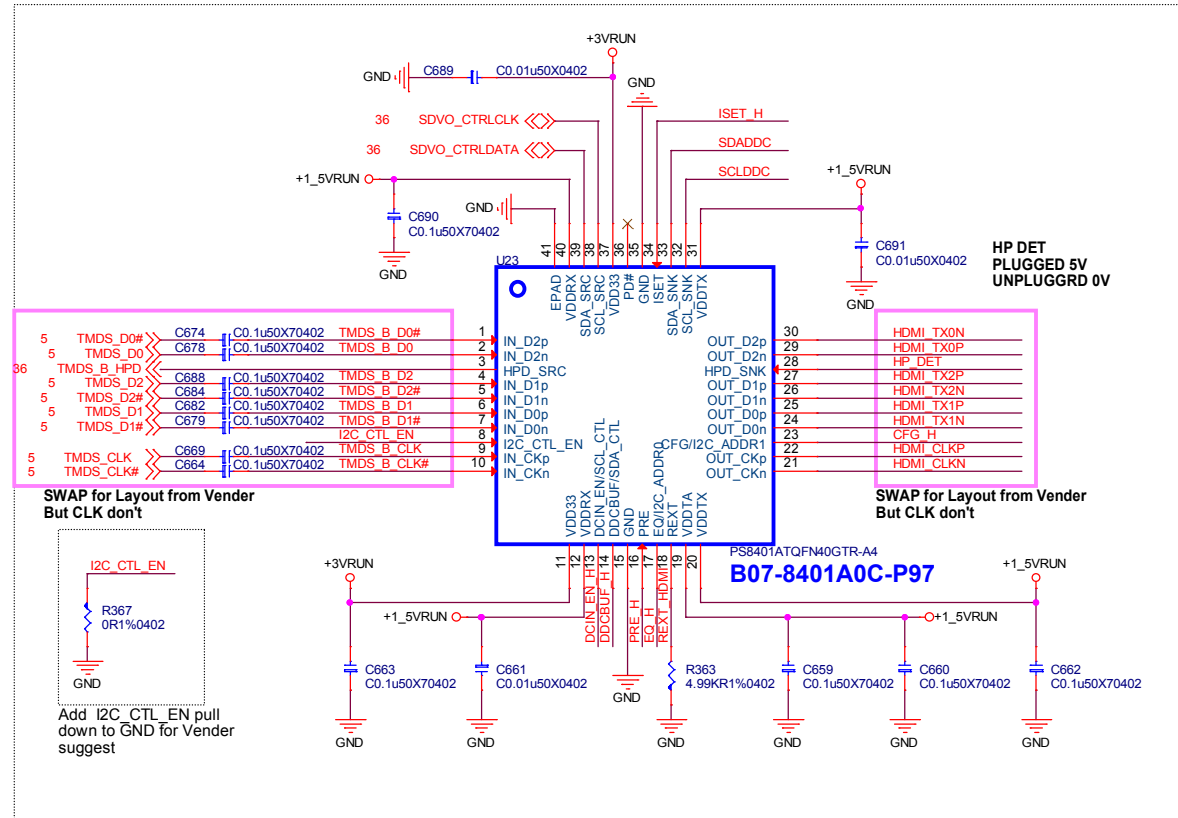
## EMI Close Connector



## Avoid DP Leakage

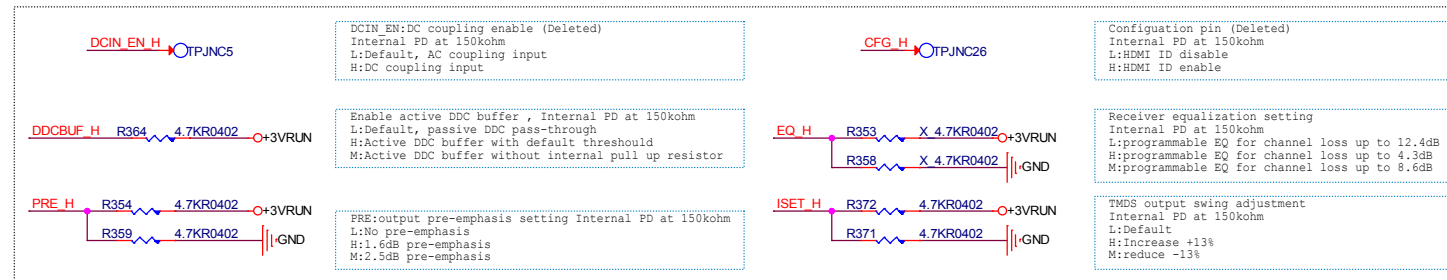
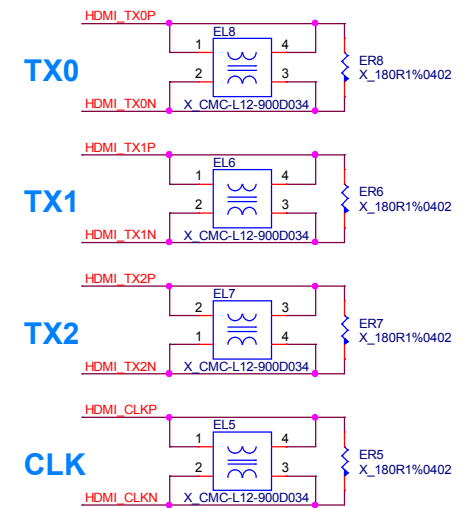


## HDMI Repeater



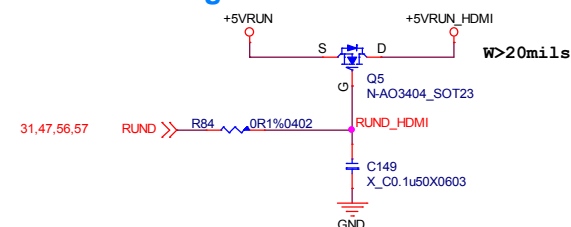
An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD\_SNK Internal PD 150kohm

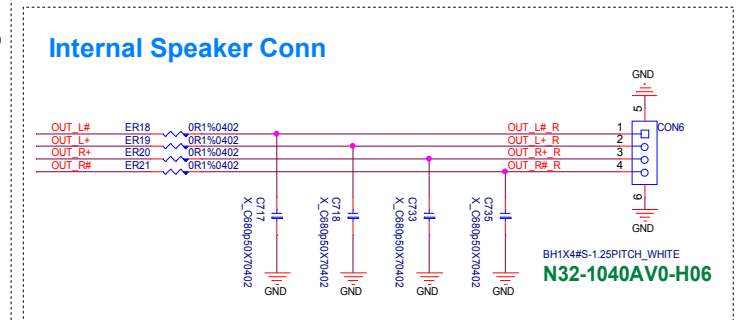
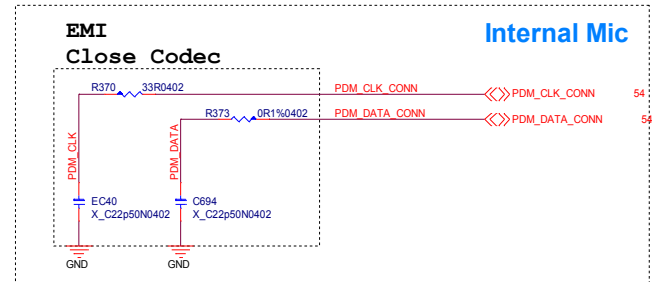
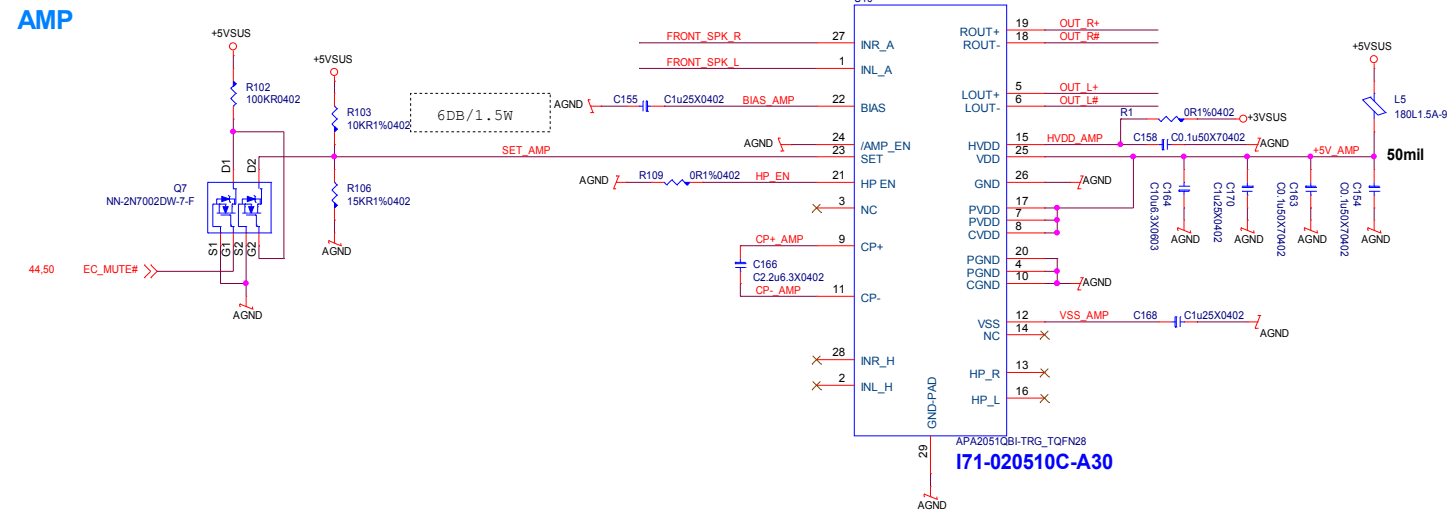
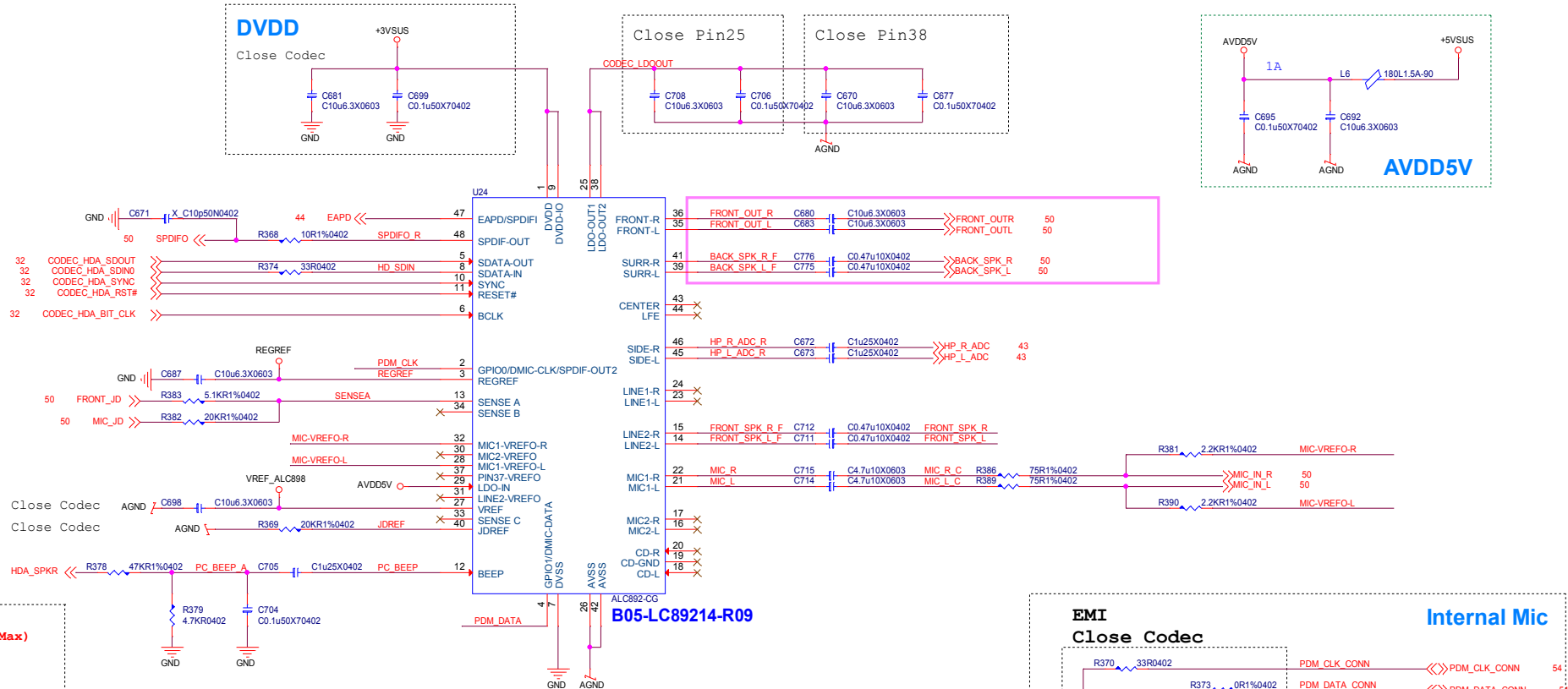
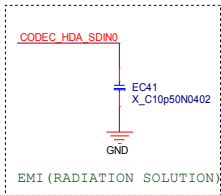
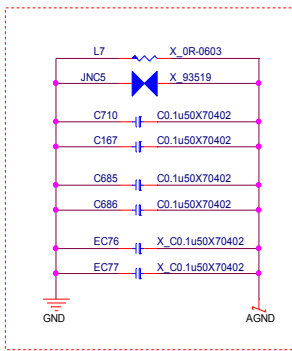


ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150k , 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

## Avoid HDMI Leakage



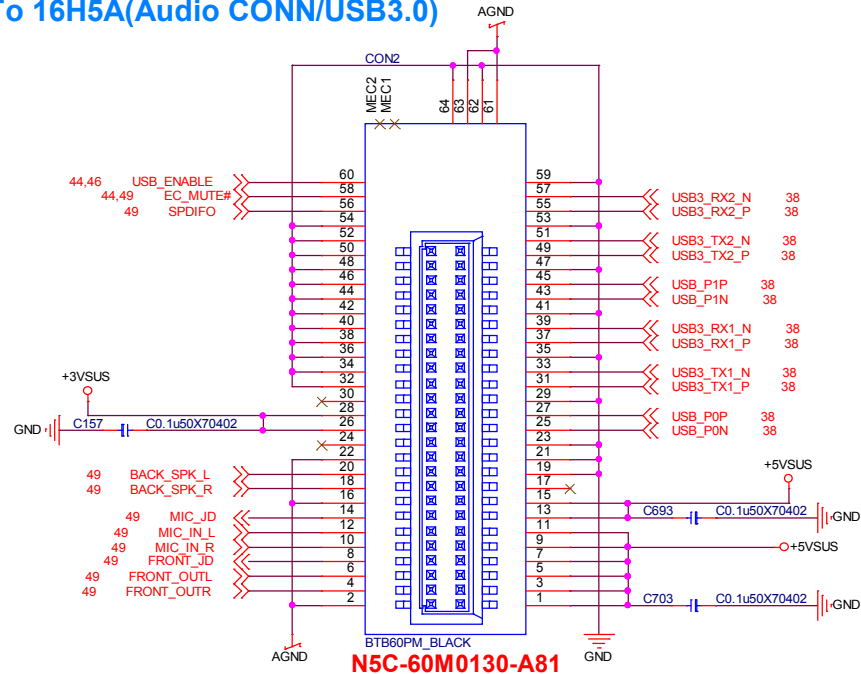
## Audio CODEC/Audio AMP



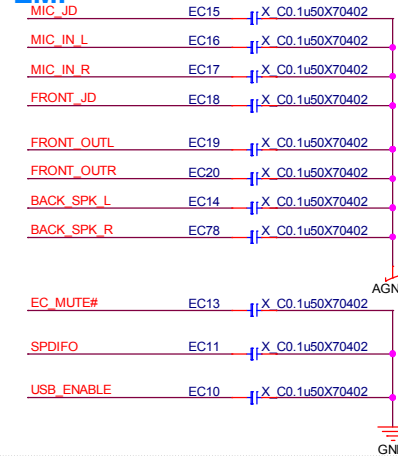


# CPU FAN/BTB CONN

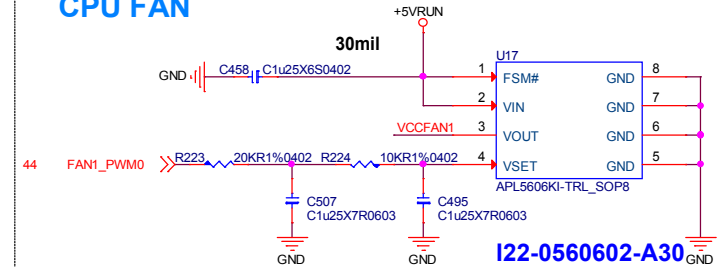
## To 16H5A(Audio CONN/USB3.0)



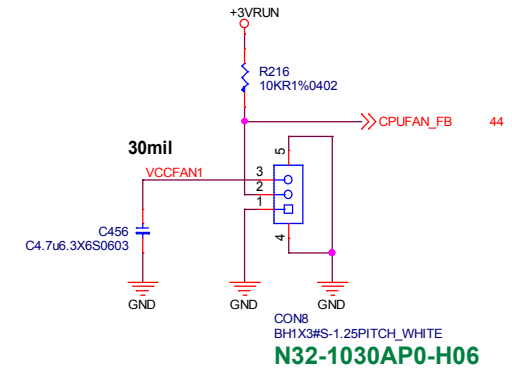
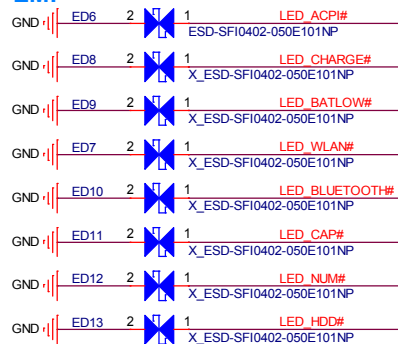
## EMI



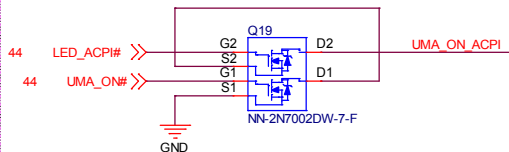
## CPU FAN



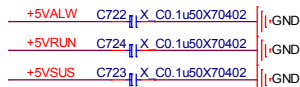
## EMI



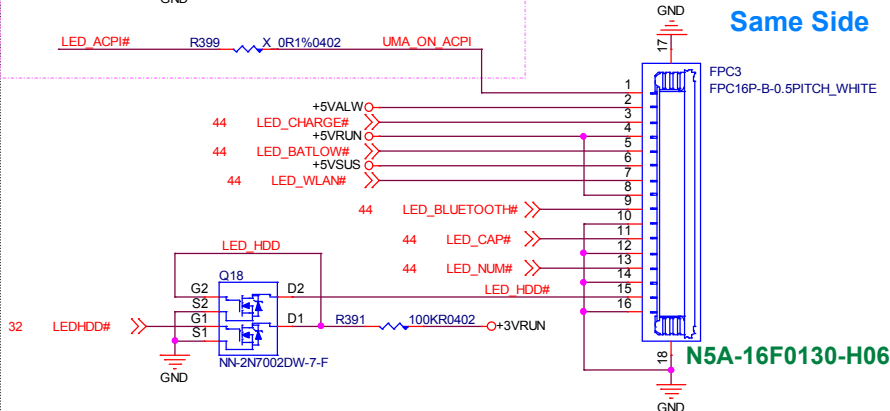
## S3 Breath S0 No active



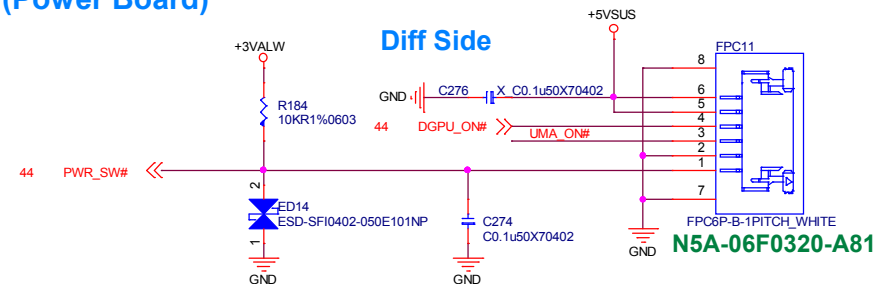
## To 16H5B(LED Board)



## Same Side



## To 16H5C (Power Board)



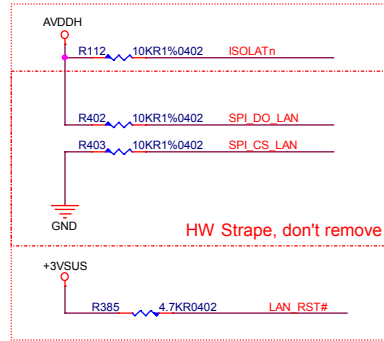
**msi**

MICRO-STAR INT'L CO.,LTD.

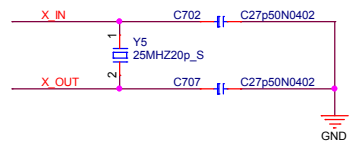
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# GIGA LAN(BigFoot BFN2205B)

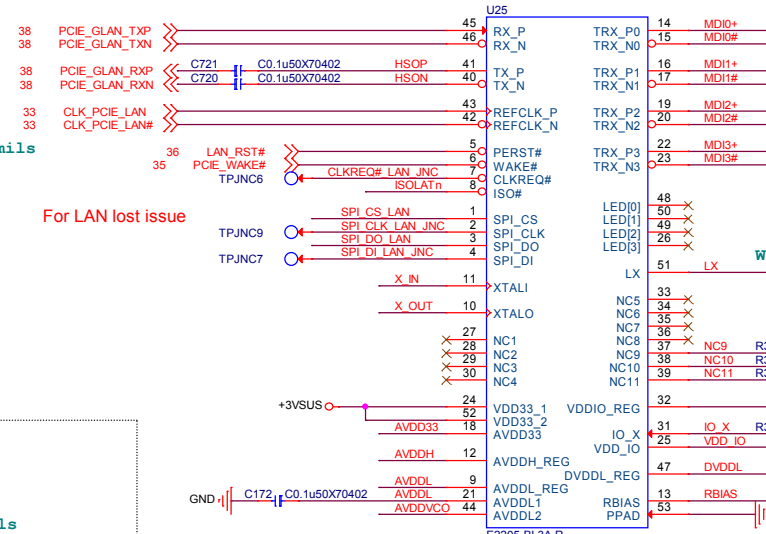
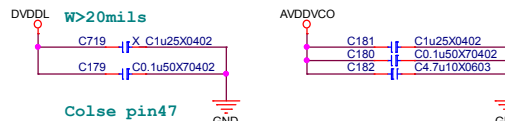
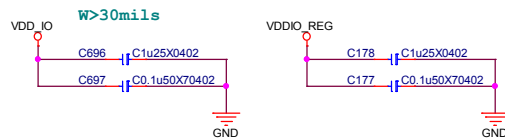
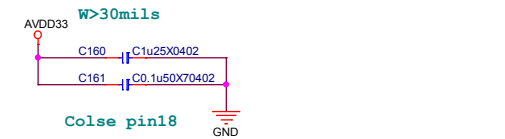
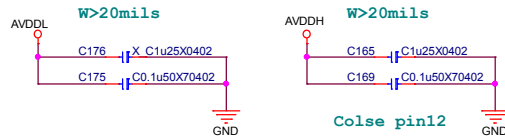


RST# spacing 20mils



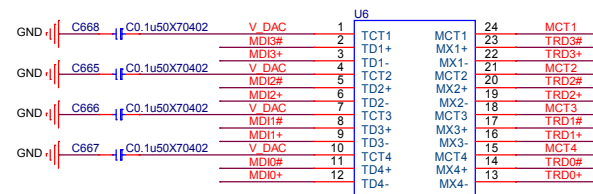
For LAN lost issue

## Power CAP

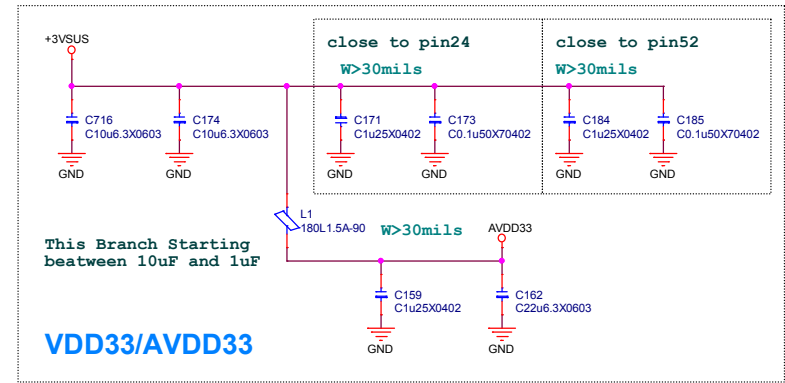
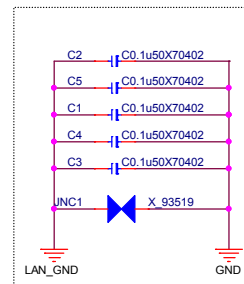
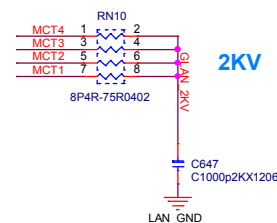


B06-E22050C-Q24

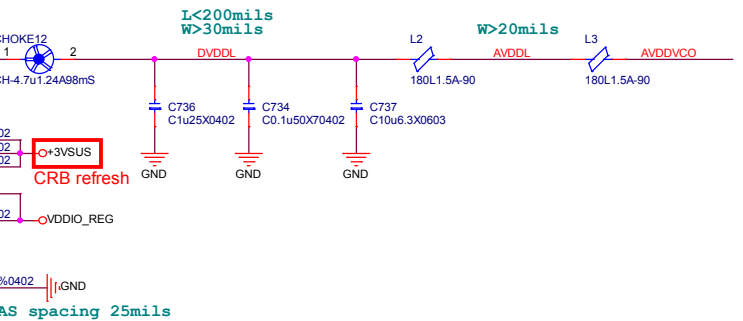
MAC 結構  
す, TQFP



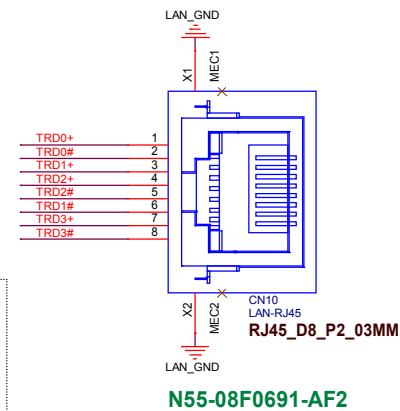
L05-0200150-B09



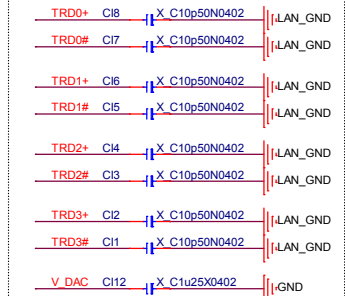
VDD33/AVDD33



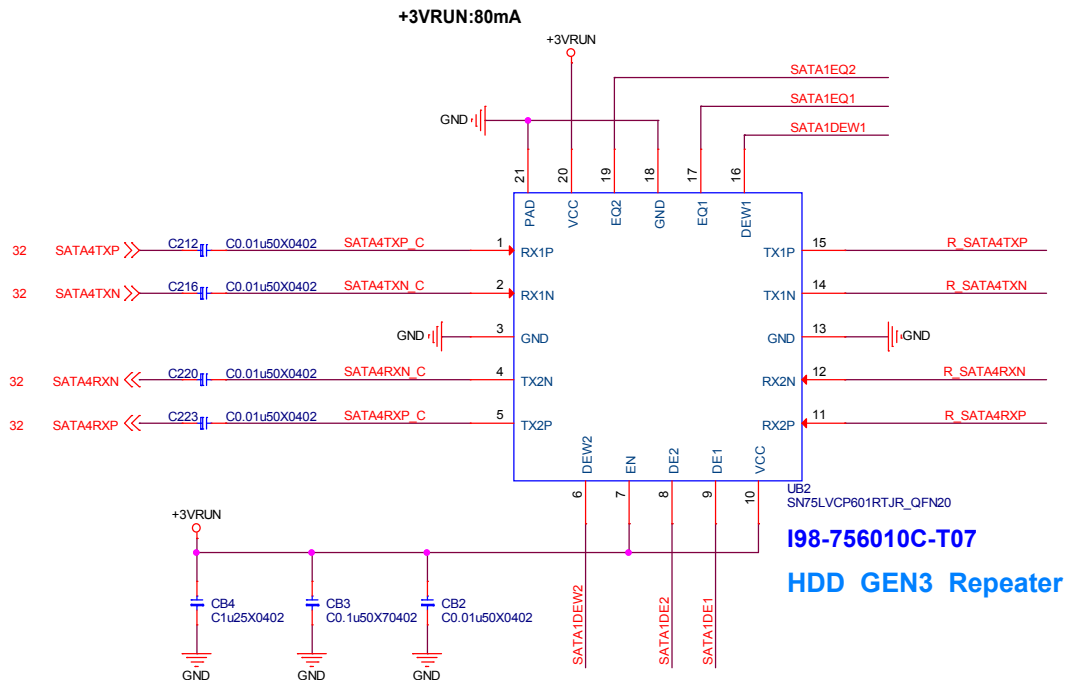
RBIAS spacing 25mils



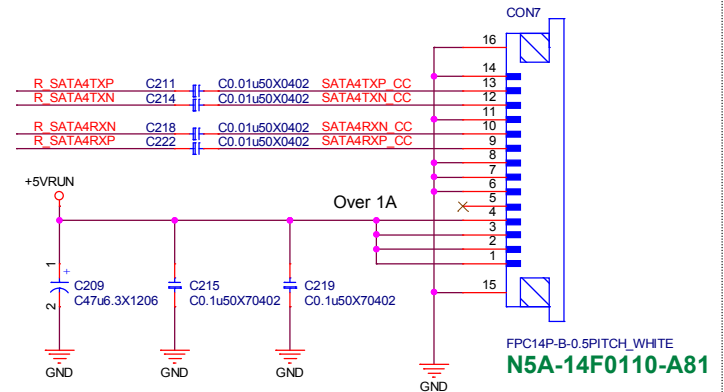
## EMI



# HDD (With Repeater)



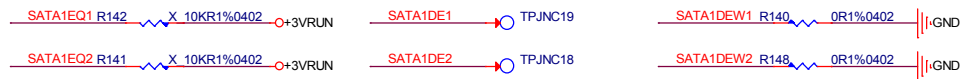
## BTB Connector



## TI SN75LVCP601RTJR HW Setting

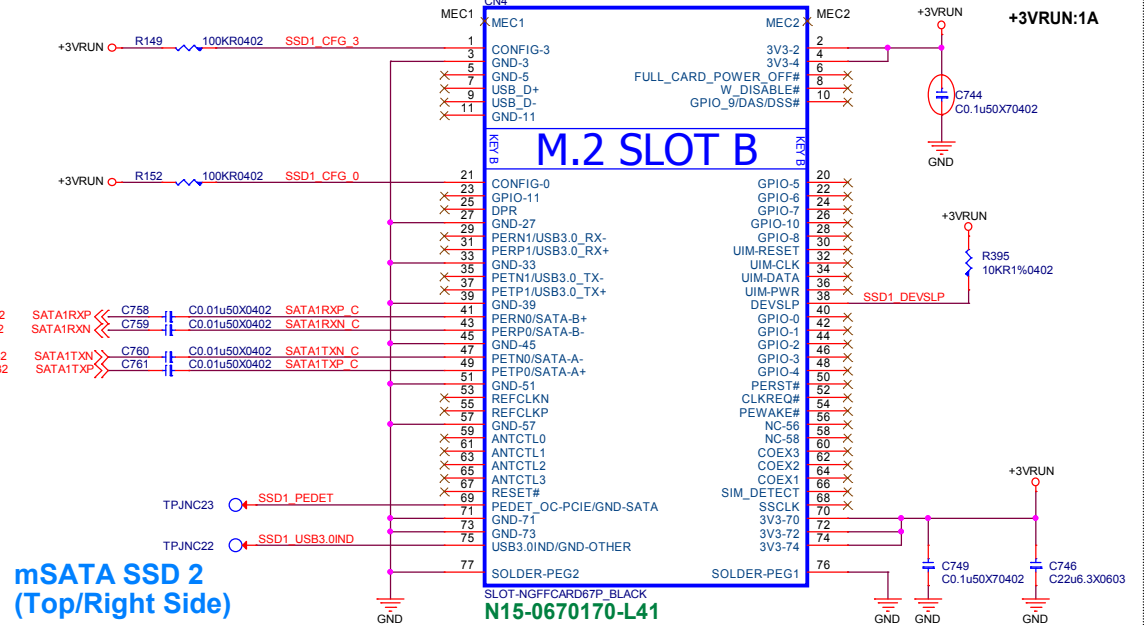
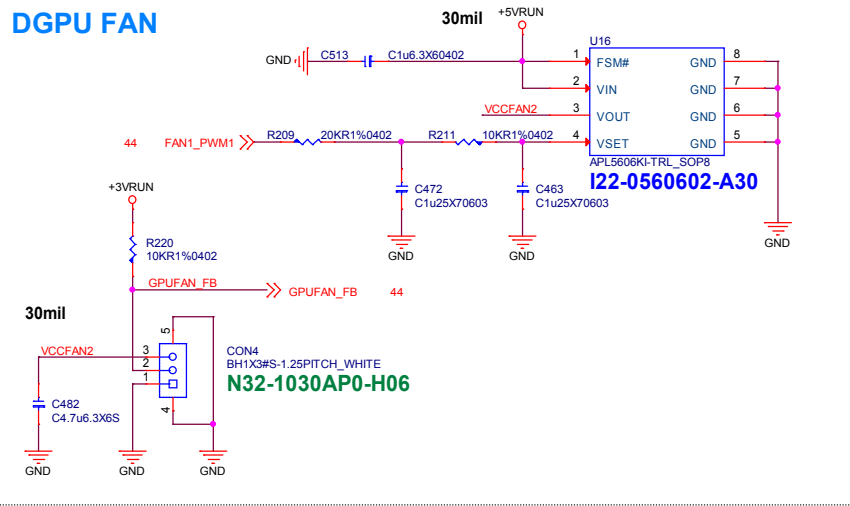
DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	DQ1/DQ2	CH1/CH2De-Emphasis dB (at 6Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)
1(default)	De-emphasis Pulse duration, long(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)

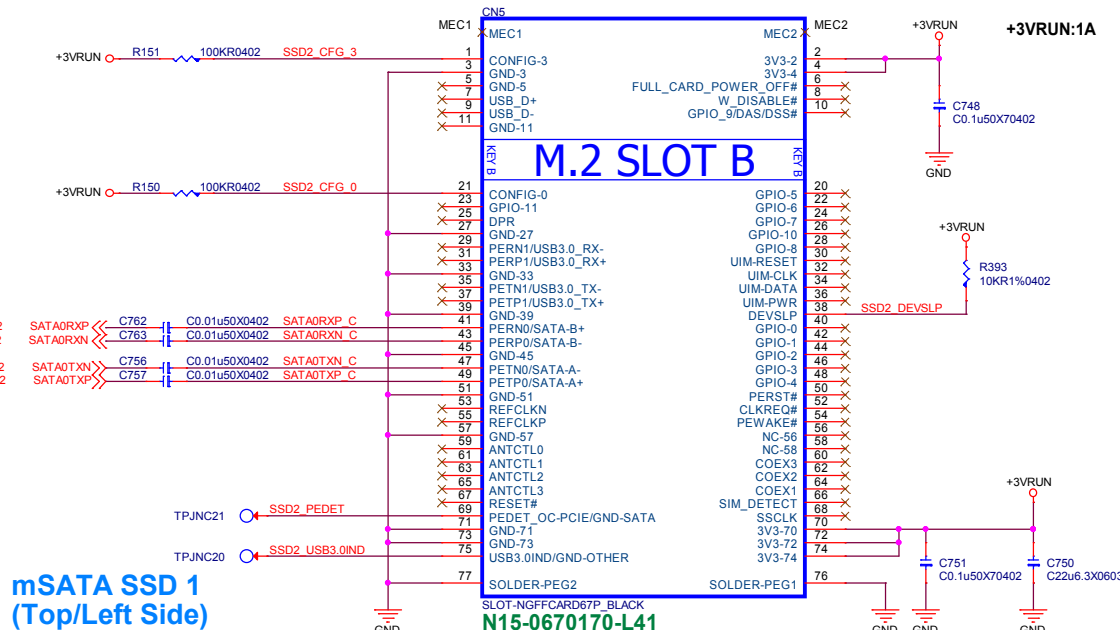


# SSD/ DGPU FAN

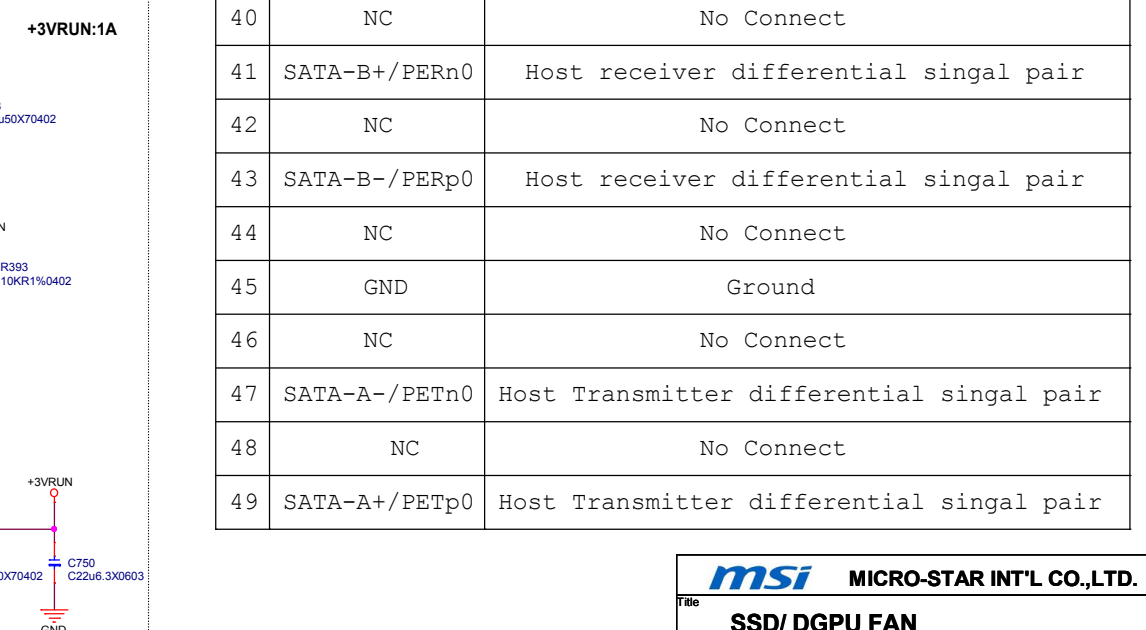
## DGPU FAN



## mSATA SSD 1 (Top/Left Side)



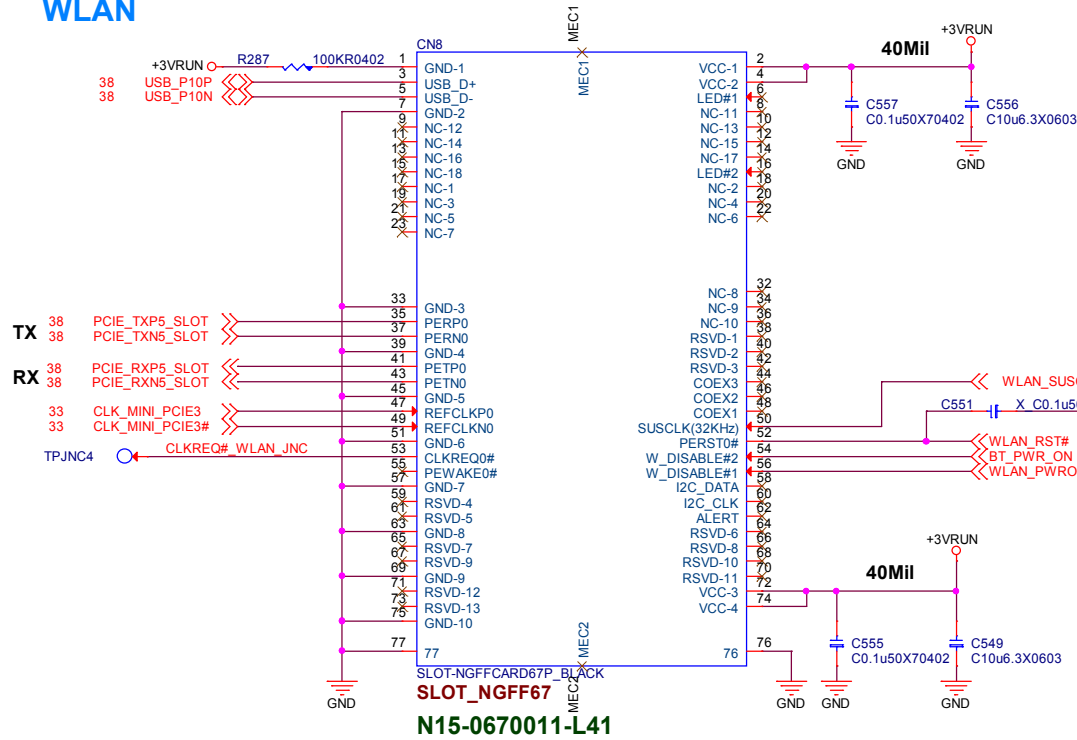
## mSATA SSD 2 (Top/Right Side)



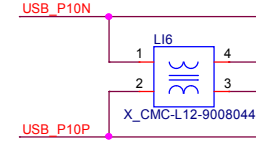
40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential singal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential singal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential singal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host Transmitter differential singal pair

# WLAN /Camera/ClickPad/FP

## WLAN

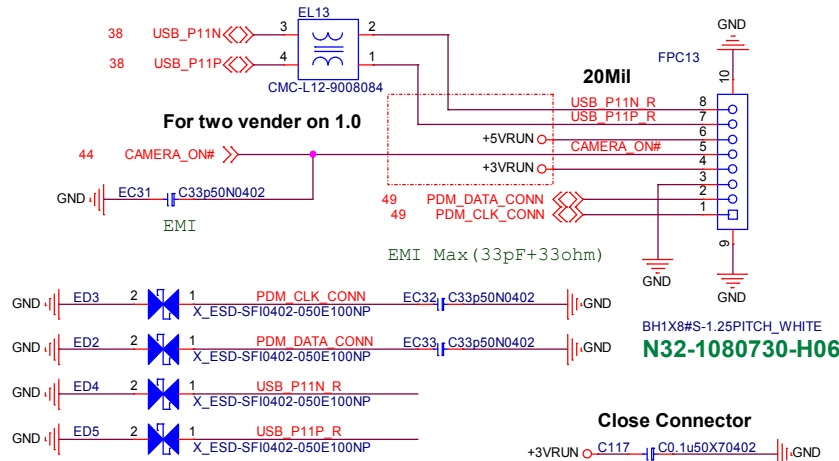


## EMI

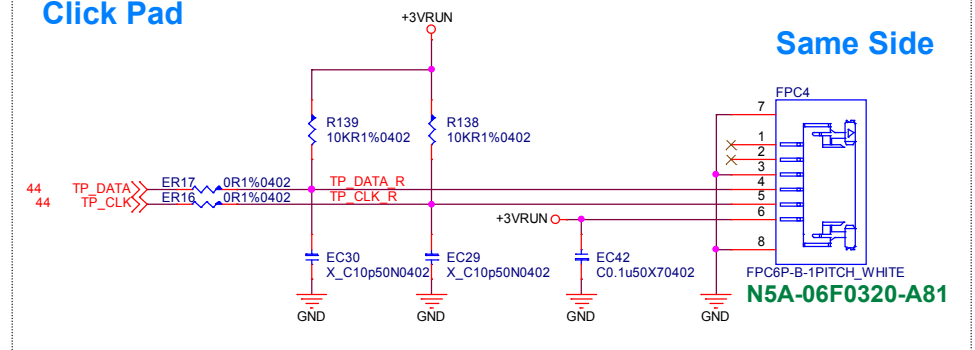


Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Reverse
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	GND	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		

## CAMERA



## Click Pad



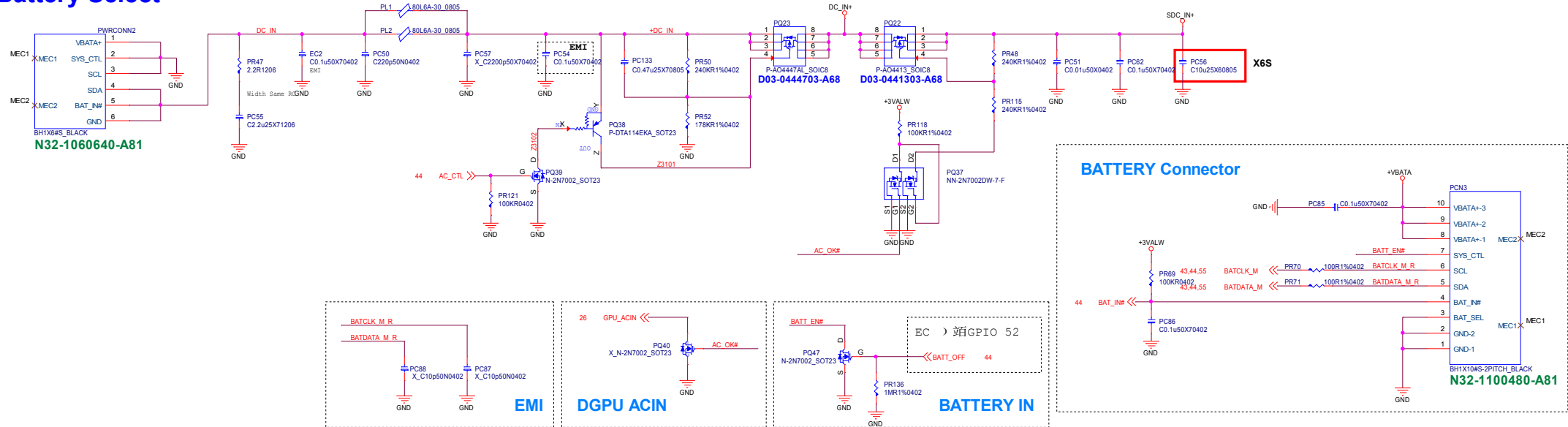
**msi**

**MICRO-STAR INT'L CO.,LTD.**

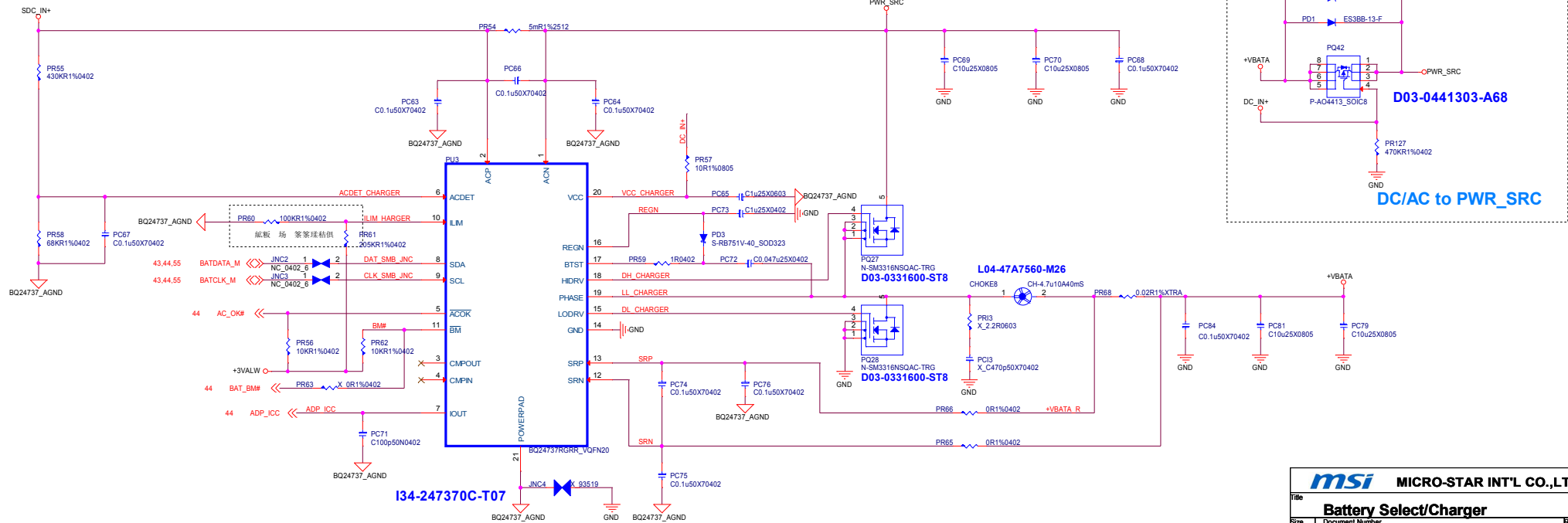
Title			WLAN /Camera/ClickPad/FP		
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## Battery Select/Charger

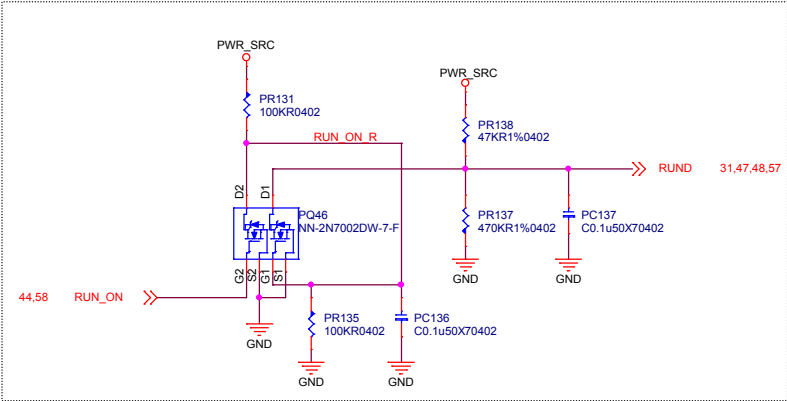
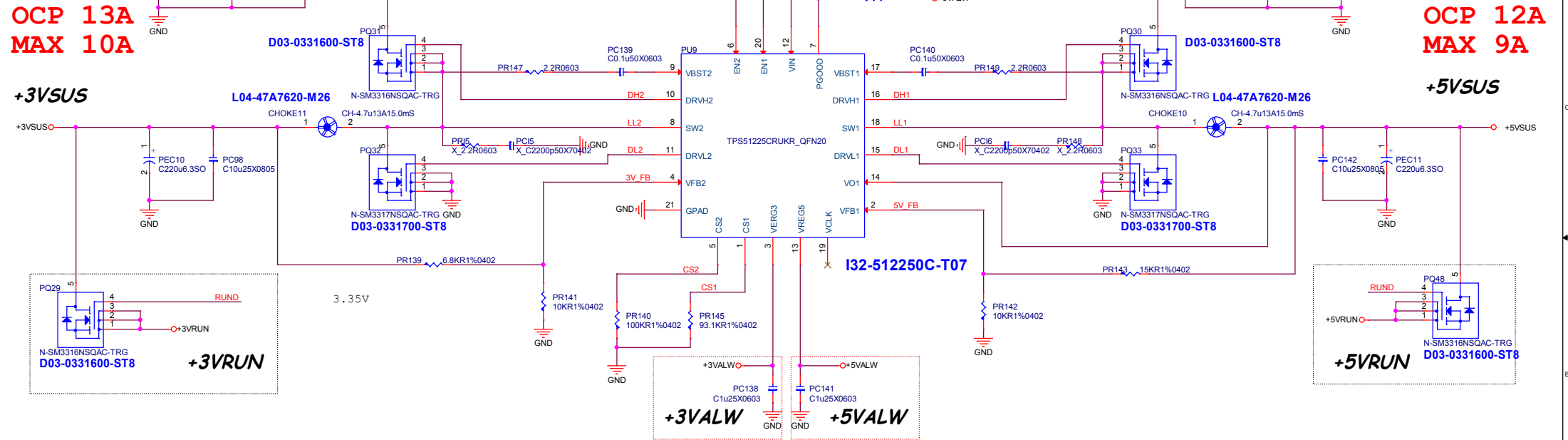
## Battery Select



## Battery Charger

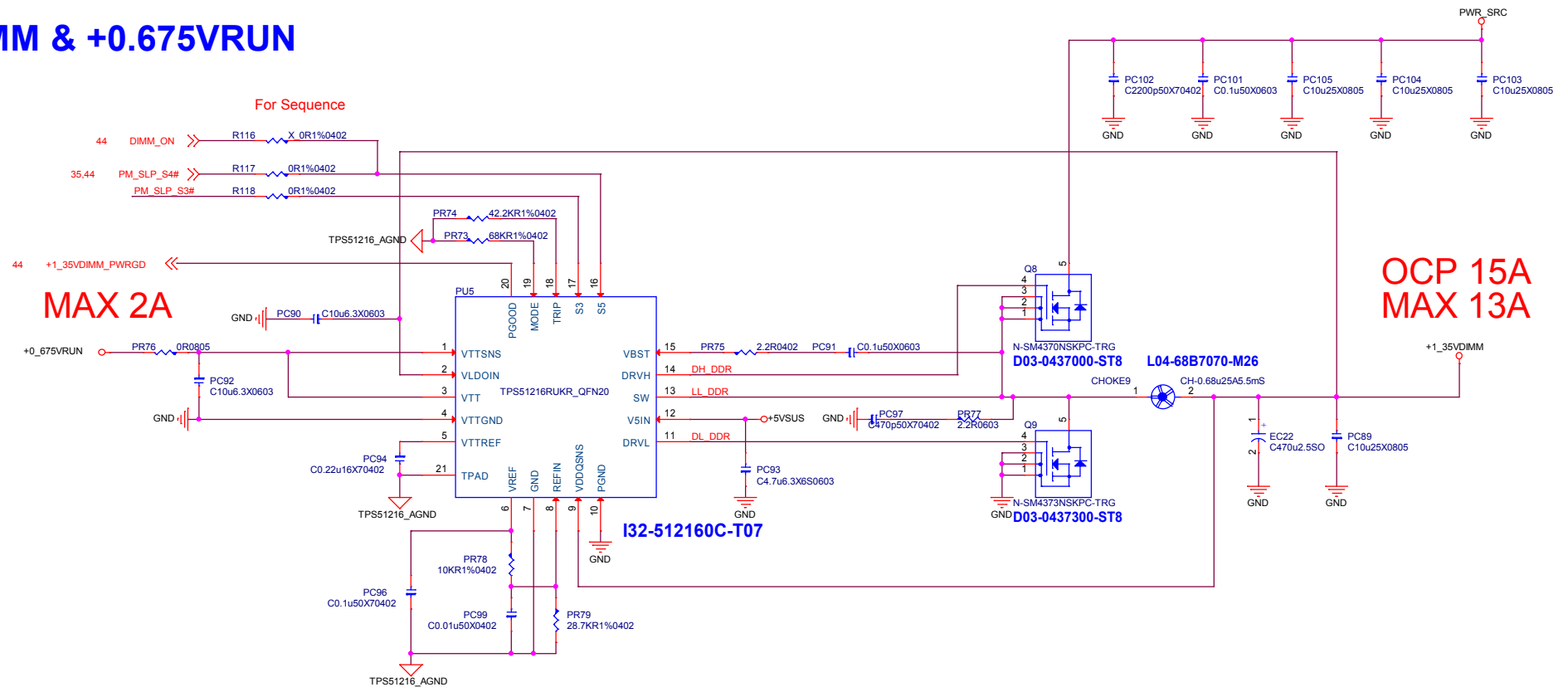


System Power

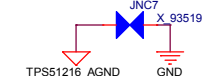
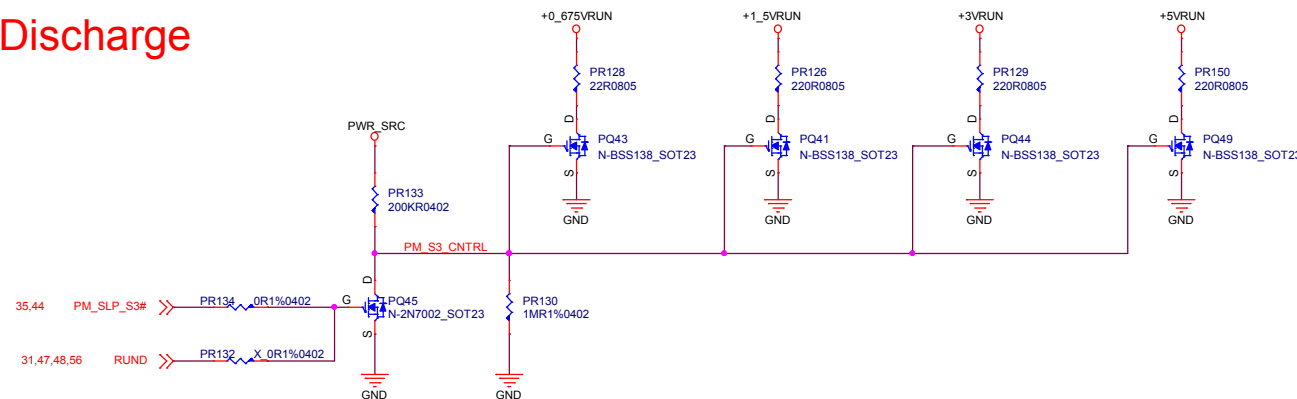


# +1.35VDIMM/+0.675VRUN

## +1.35VDIMM & +0.675VRUN



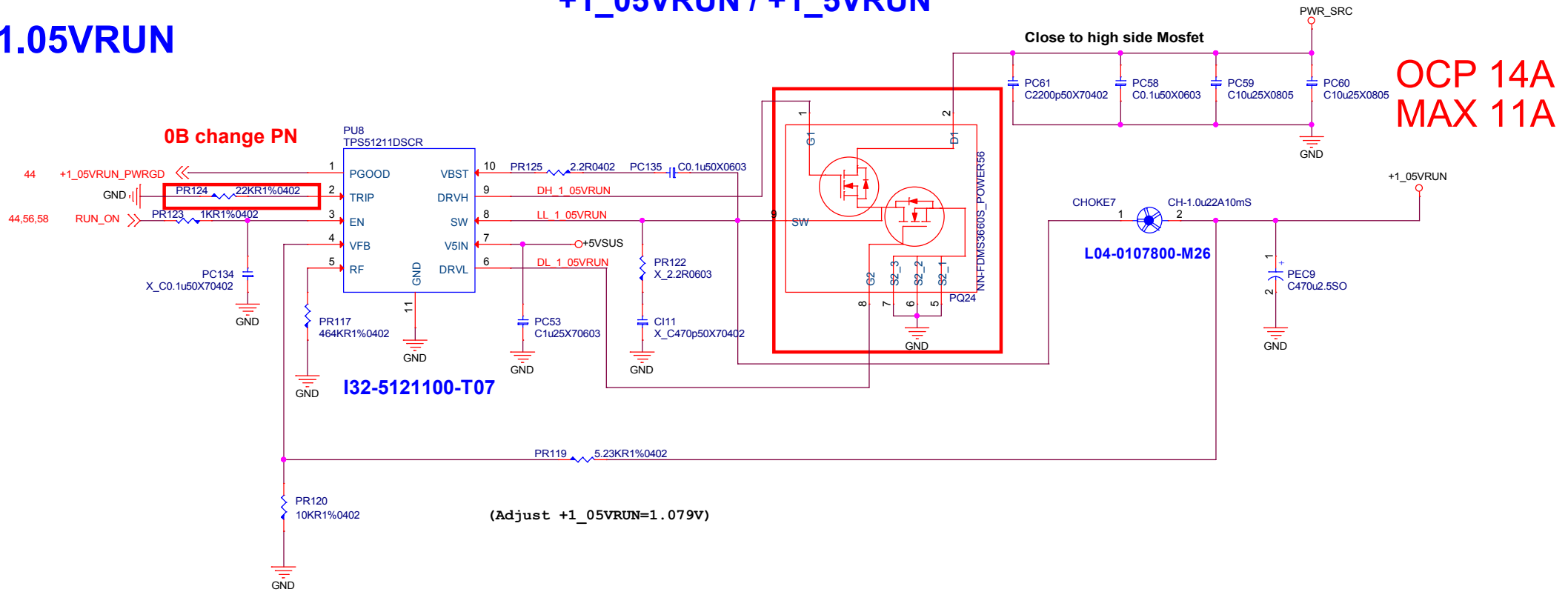
## Discharge





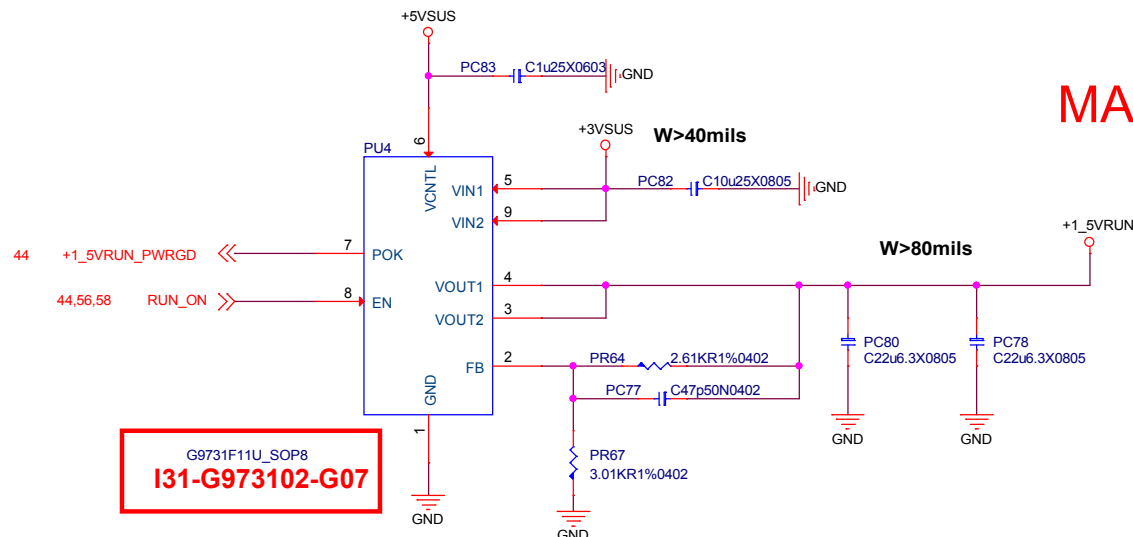
+1.05VRUN


+1\_05VRUN / +1\_5VRUN



+1.5VRUN

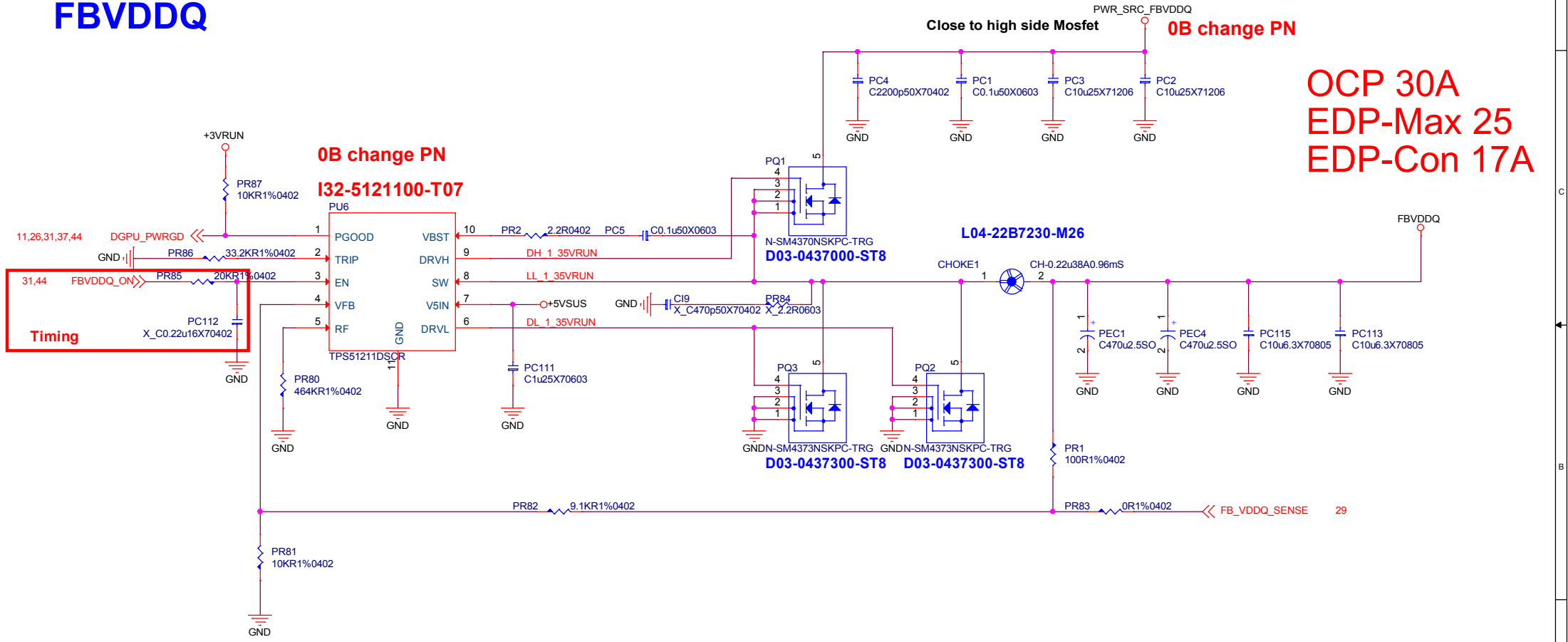
MAX 2A



		MICRO-STAR INT'L CO.,LTD.	
Title			
+1_05VRUN / +1_5VRUN			
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# DGPU POWER FBVDDQ

## FBVDDQ

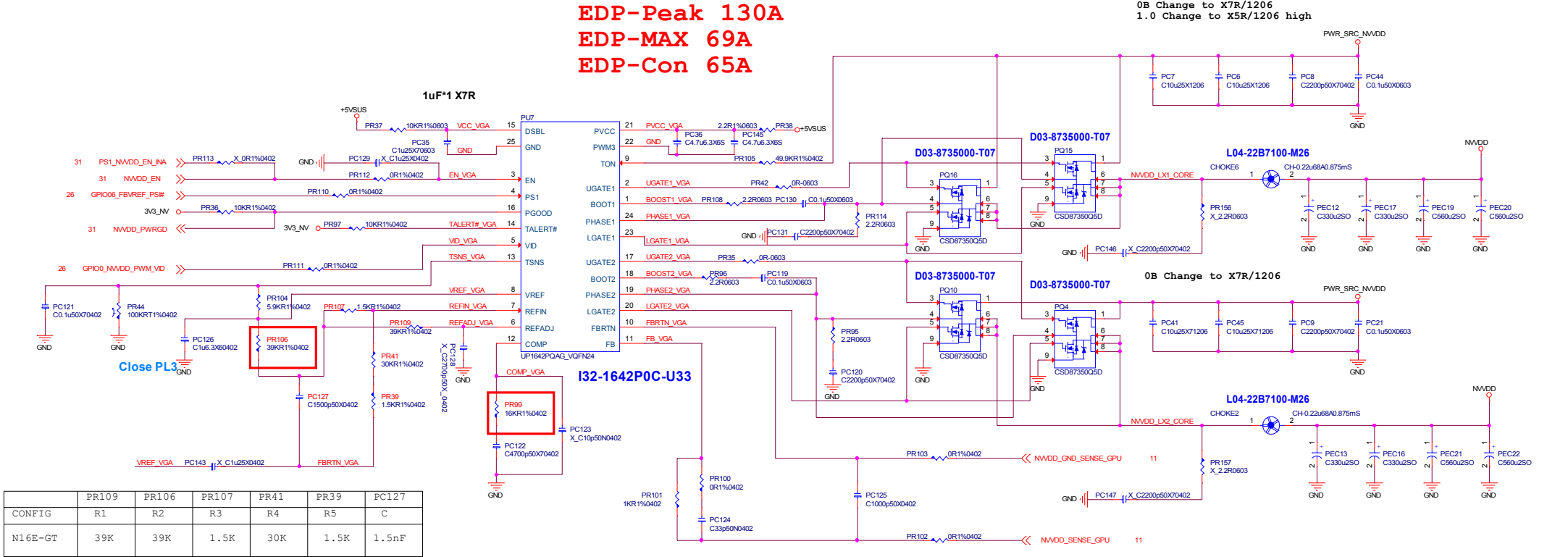


DGPU POWER NVVDD

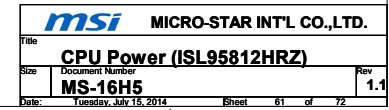
DGPU POWER / UP1642PQAG

CONFIG B  
VBoot:0.9V  
Vmin:0.6V / Vmax:1.2V

EDP-Peak 130A  
EDP-MAX 69A  
EDP-Con 65A

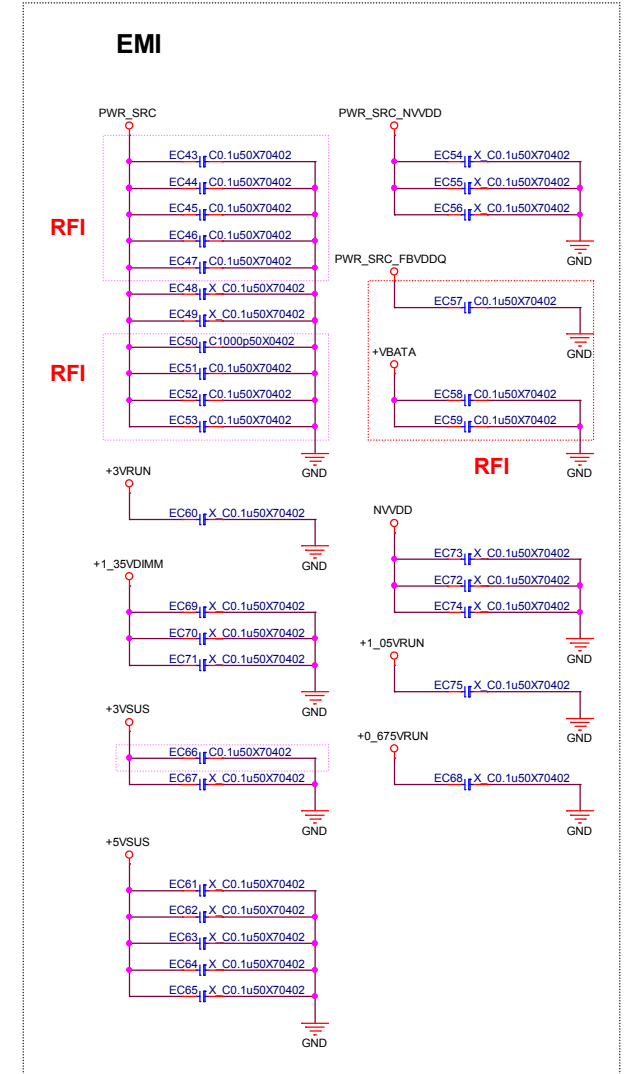
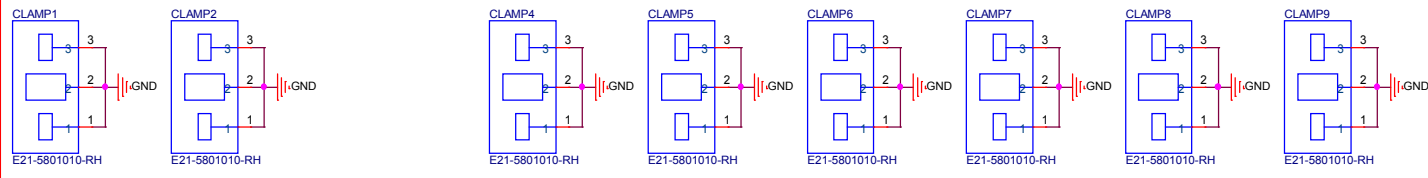
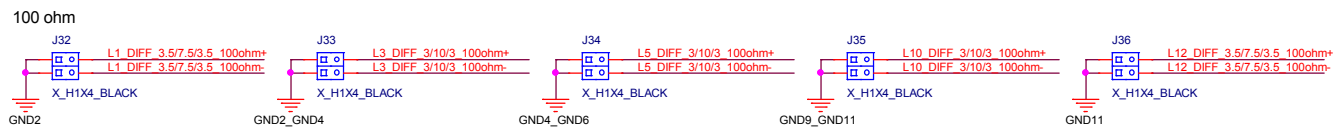
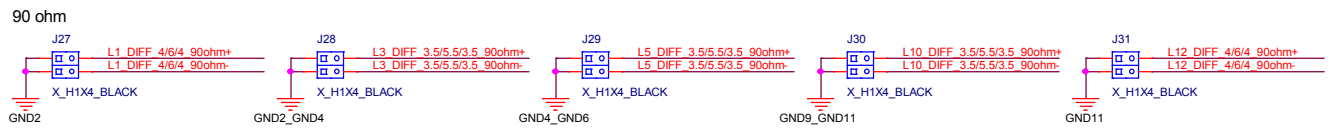
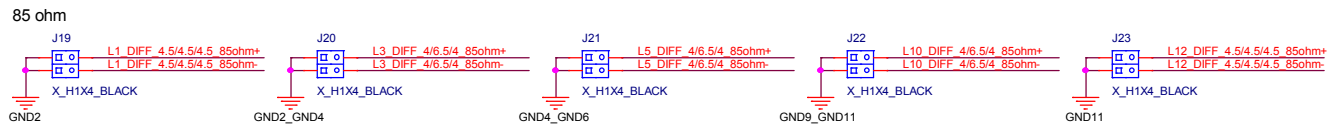
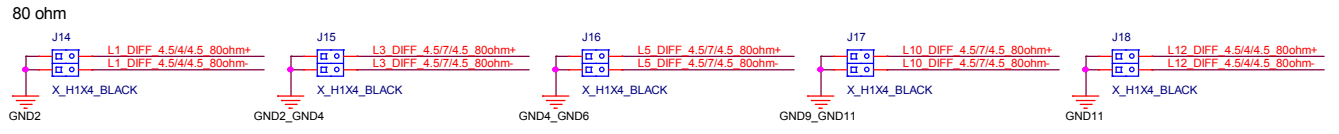
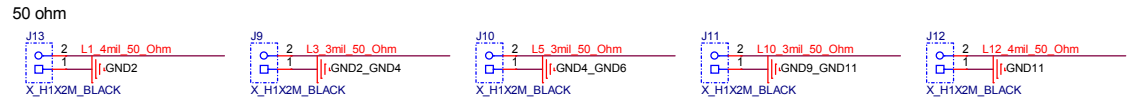
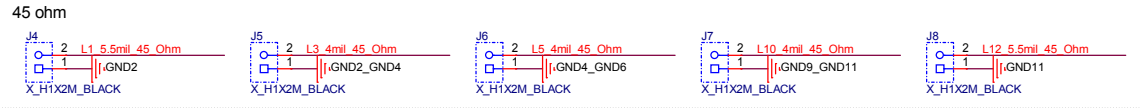


MAX 95A  
TDC 27A

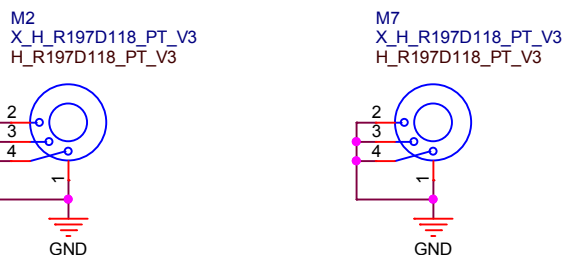
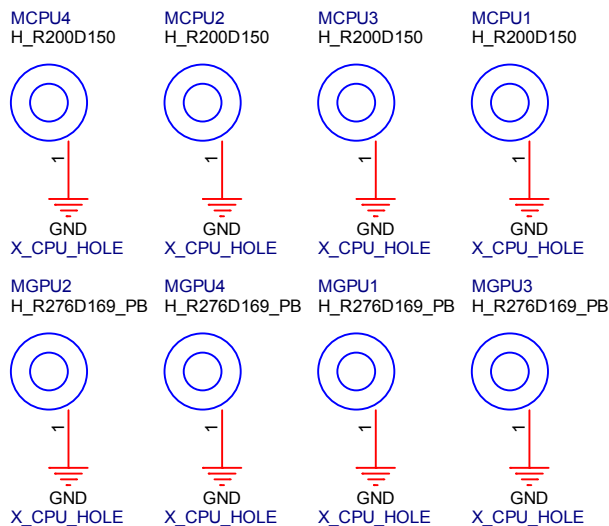


# EMI/ Impedance

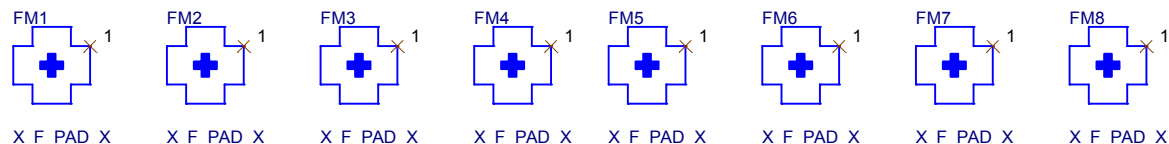
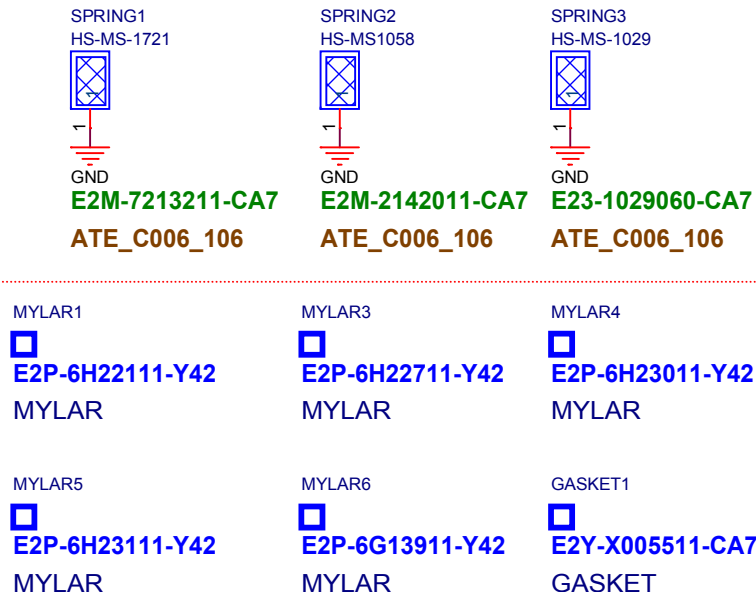
## Impedance Connector No PN



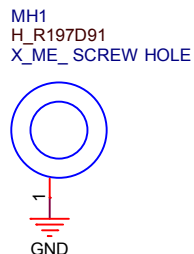
## CPU/GPU Holes



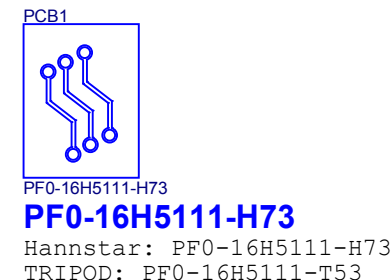
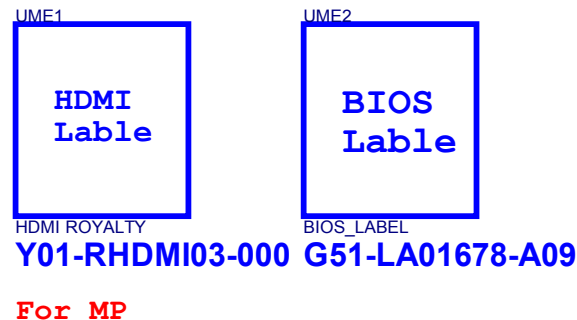
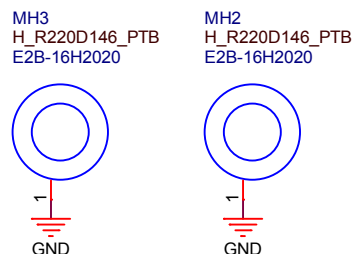
## EMI



## Fan Hole



## SSD Stand off



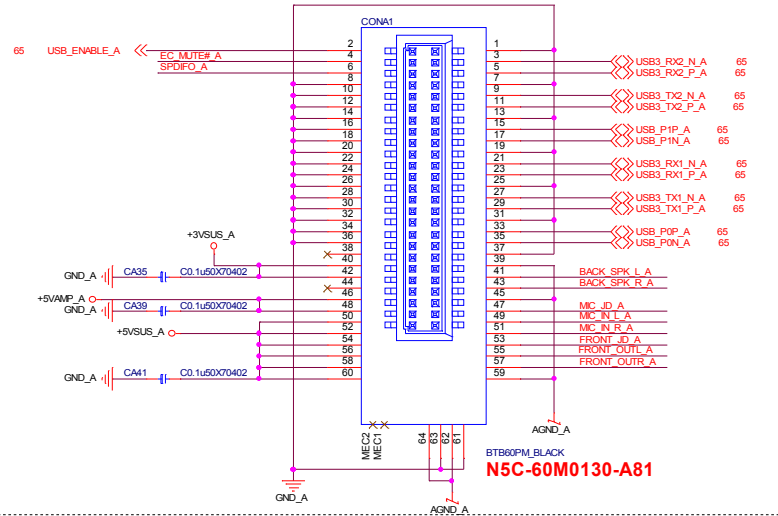
**msi**

**MICRO-STAR INT'L CO.,LTD.**

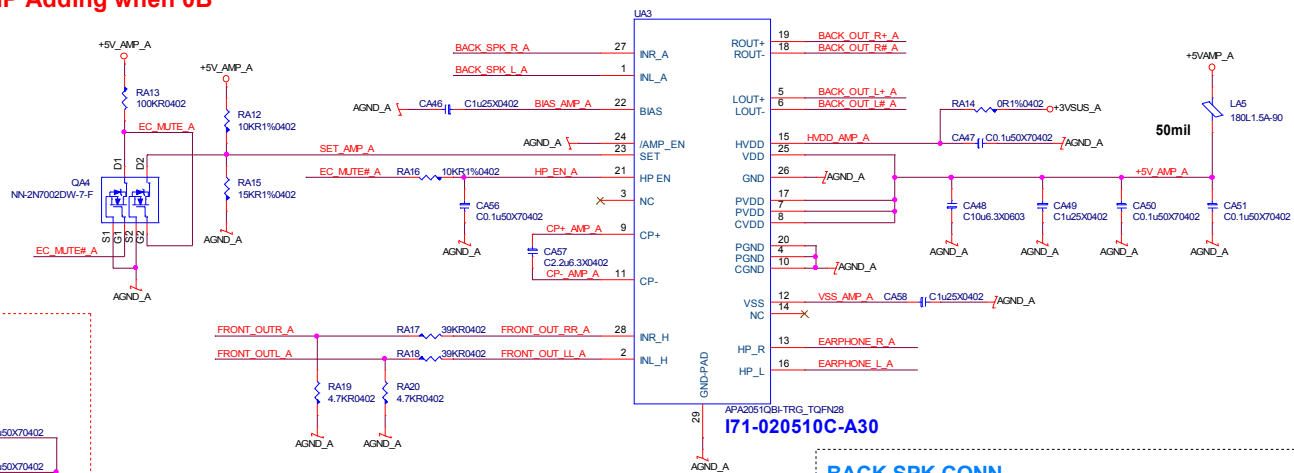
Title		Screw/ME	
Size	Document Number	Rev	
	<b>MS-16H5</b>	<b>1.1</b>	
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## 16H5-A Board (Audio CONN)

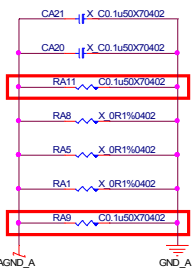
**BTB Connector From MB**  
CONN Pin Current Capability : 0.5A/Pin



## AMP Adding when 0B



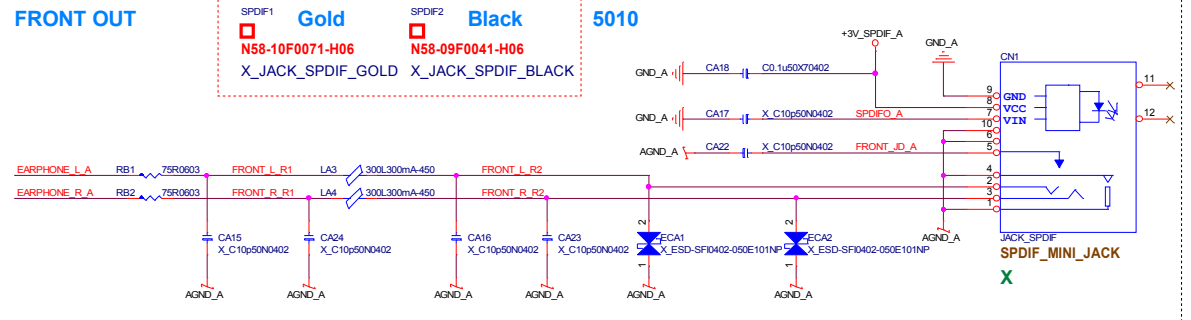
## EMI



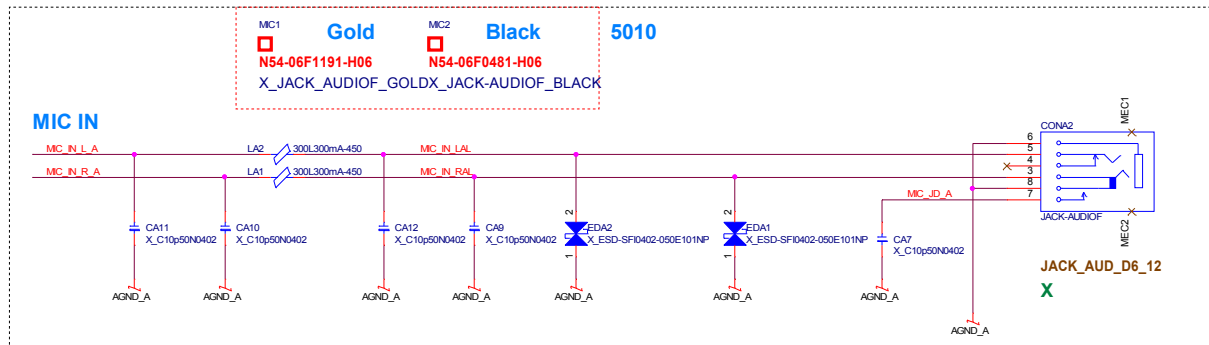
## Change to Cap

## Change to Cap

**FRONT OUT**



**MIC IN**

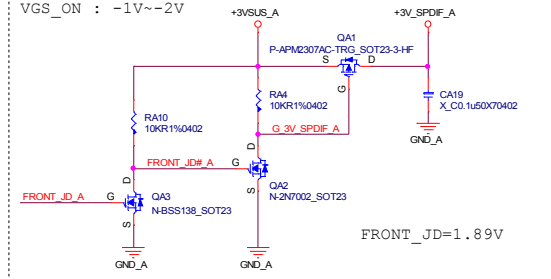


## SPDIF Power

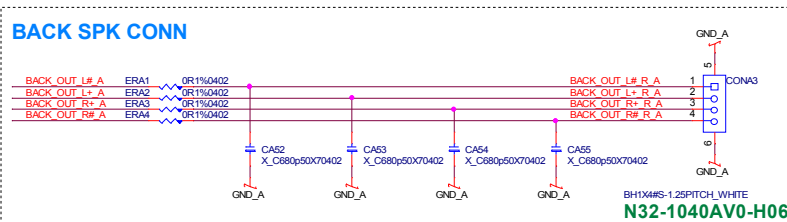
```

| VGS_ON  : -1V~-2V

```

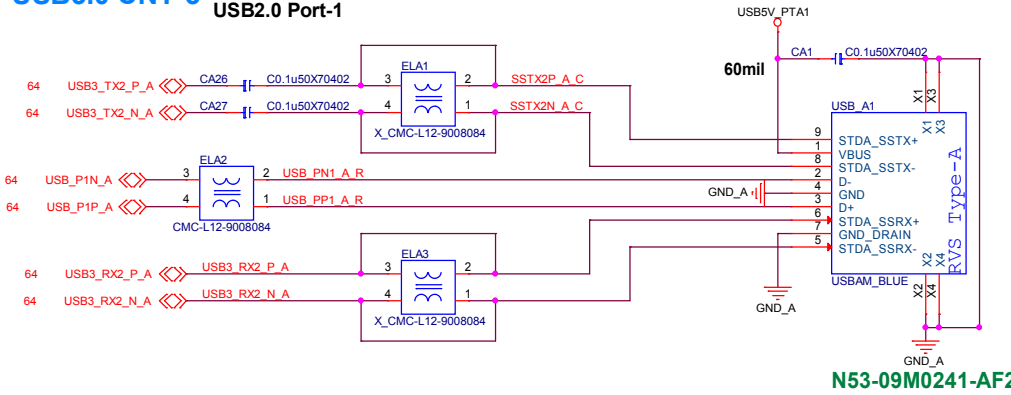


**BACK SPK CONN**

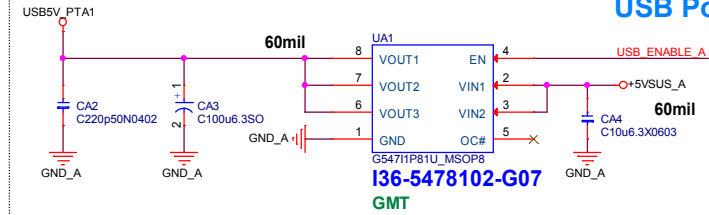


# [A] USB3.0 CNT-2/-3

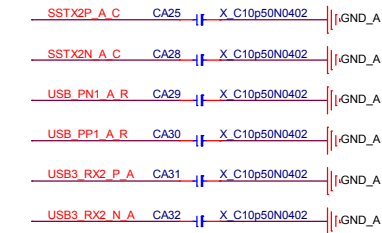
## USB3.0 CNT-3 USB3.0 Port-2 USB2.0 Port-1



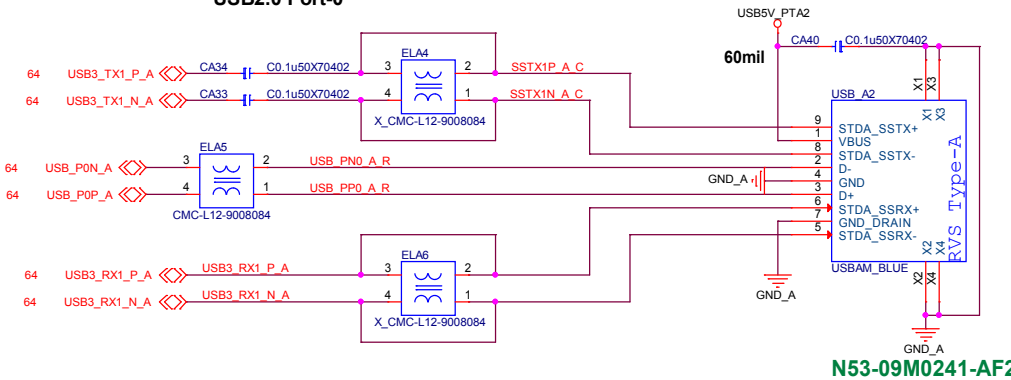
## USB Power Switch



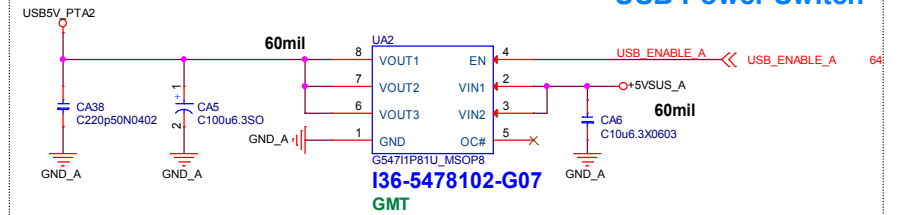
## EMI



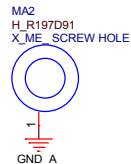
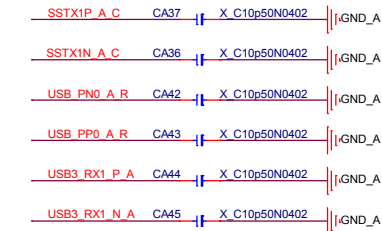
## USB3.0 CNT-4 USB3.0 Port-1 USB2.0 Port-0



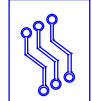
## USB Power Switch



## EMI



PCBA1



PF0-16H5A11-H73

Hannstar: PF0-16H5A11-H73

TRIPOD: PF0-16H5A11-T53

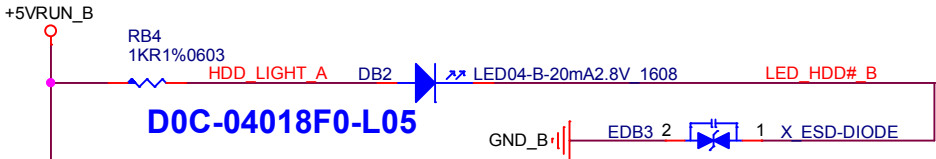
MYLARA1	MYLARA2
E2P-6H22812-G40	E2P-6H22311-G40
MYLAR	MYLAR



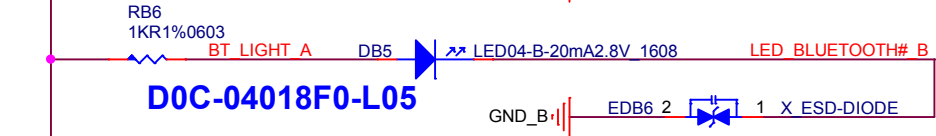
16H5-B Board (LED Board)

LED

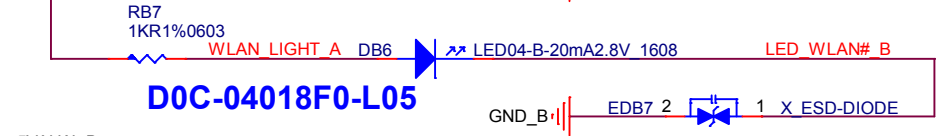
BLUE  
(HDD)



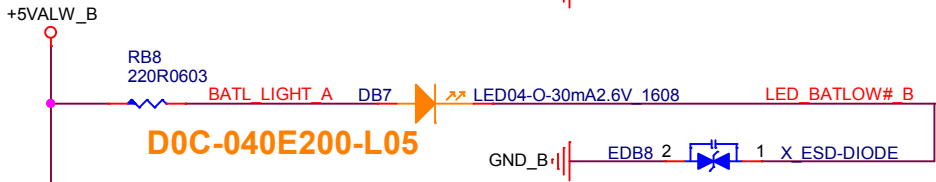
BLUE  
(BT)



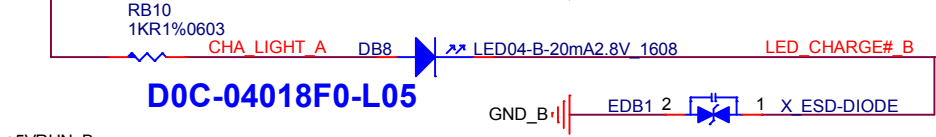
BLUE  
(WLAN)



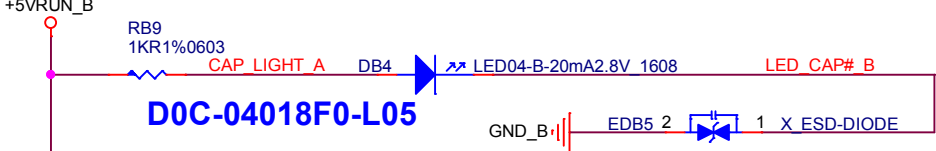
ORANGE  
(BATLOW)



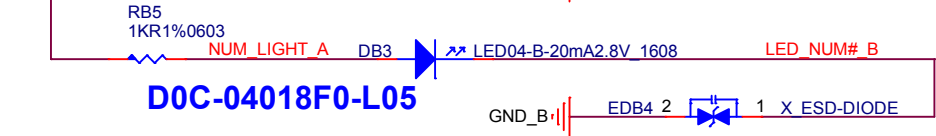
BLUE  
(CHARGE)



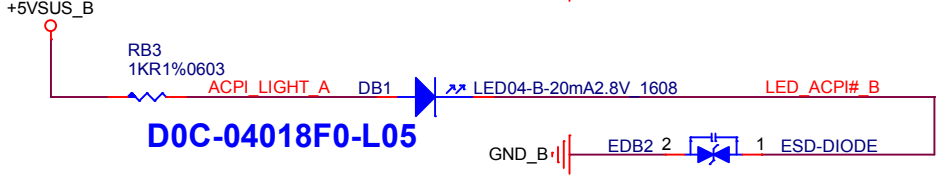
BLUE  
(CAP)



BLUE  
(NUM)

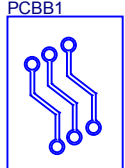
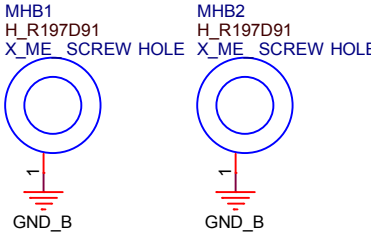
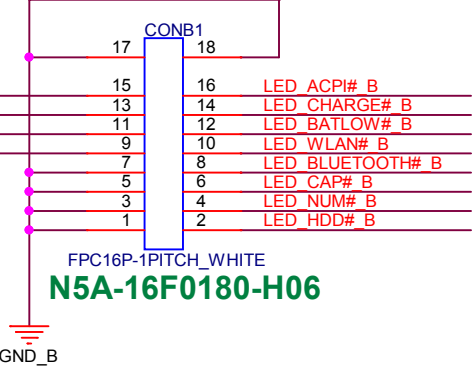


BLUE  
(ACPI)



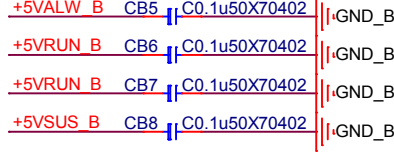
Connector

Same Side



PF0-16H5B11-H73  
PF0-16H5B11-H73

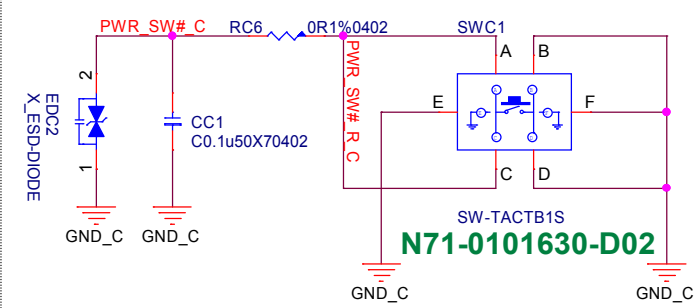
Hannstar: PF0-16H5B11-H73  
TRIPOD: PF0-16H5B11-T53



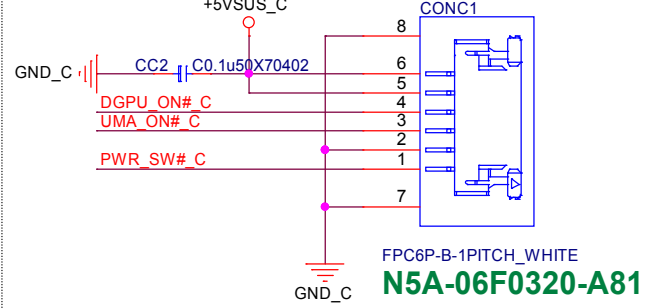
msi MICRO-STAR INT'L CO.,LTD.			
Title			
LED Board			
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# 16H5-C Board (Power SW Board)

## Power Switch

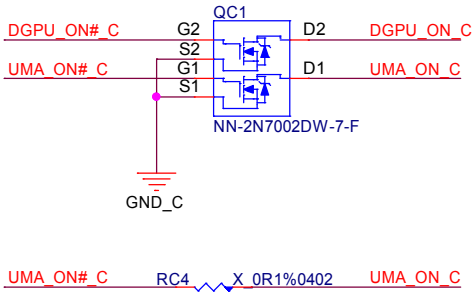


## Diff Side Connector

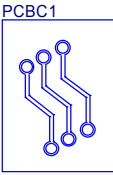
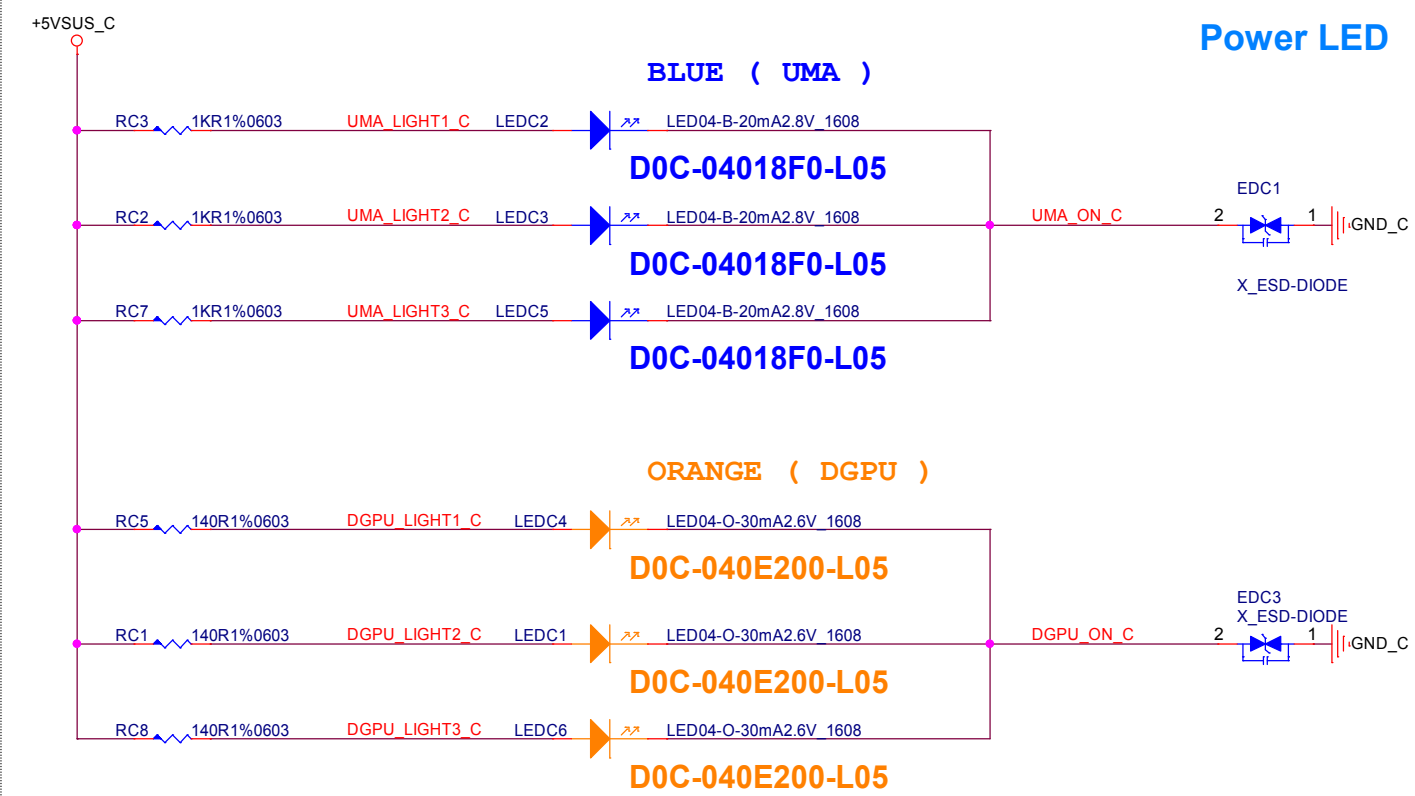


## UMA/DGPU Logic

MOS Ton, Toff 20ns



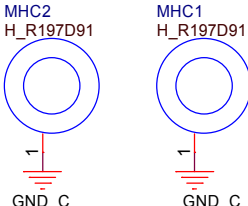
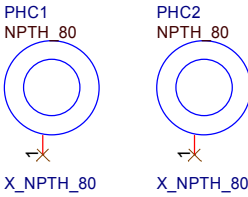
## Power LED




PF0-16H5C11-H73

Hannstar: PF0-16H5C11-H73

TRIPOD: PF0-16H5C11-T53

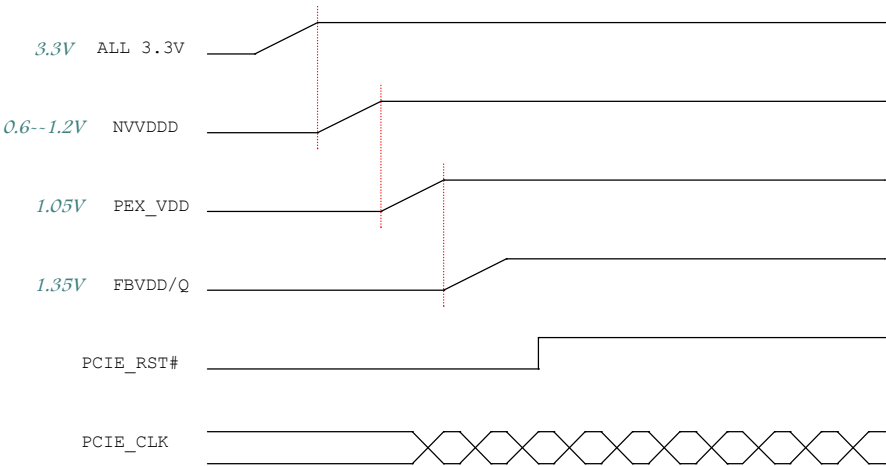


X\_ME\_SCREW HOLE X\_ME\_SCREW HOLE

		MICRO-STAR INT'L CO.,LTD.	
Title			
Power SW Board			
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2		1	

# MS-16H5 DGPU POWER SEQUENCE

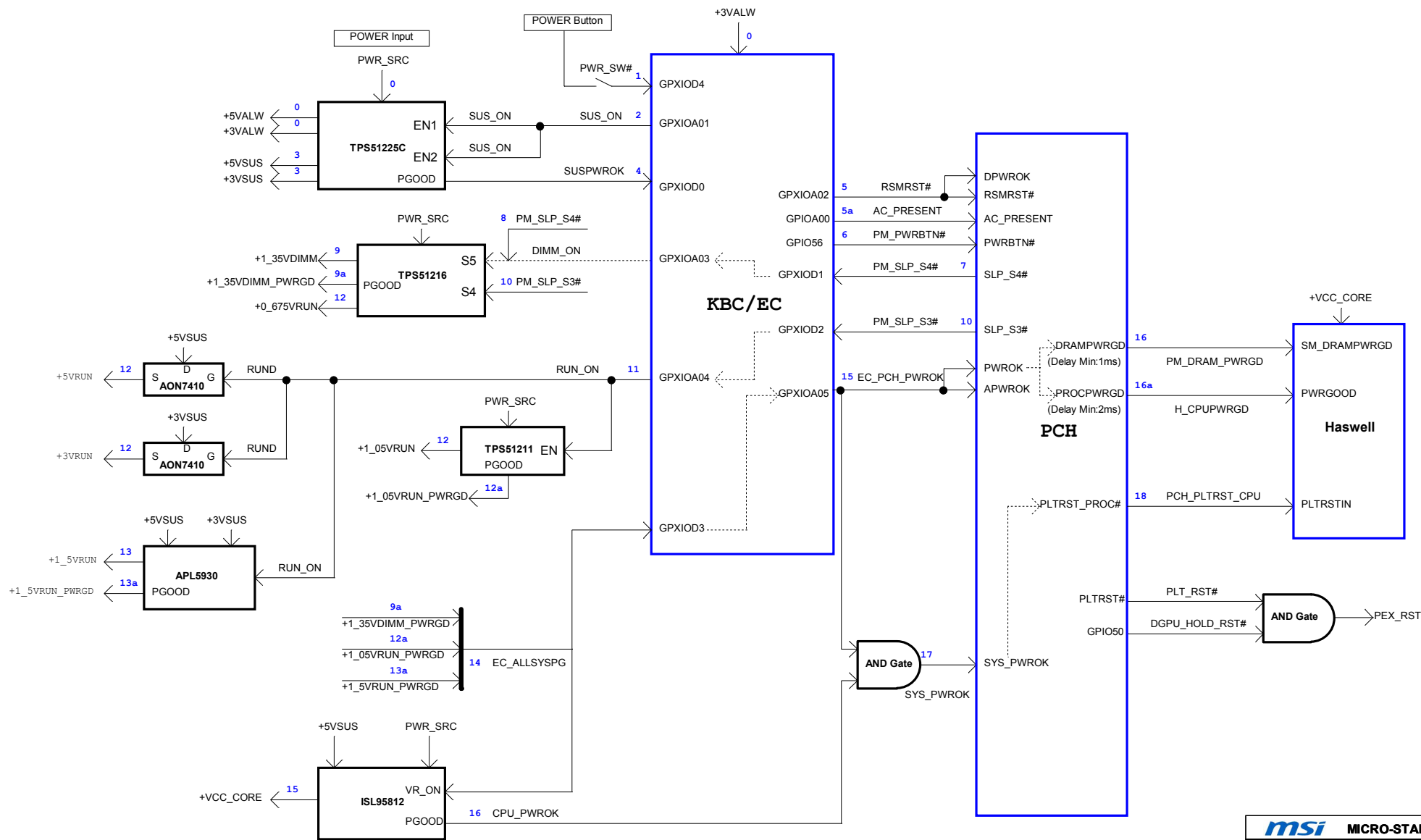
GPU POWER ON SEQUENCE



NOTES:

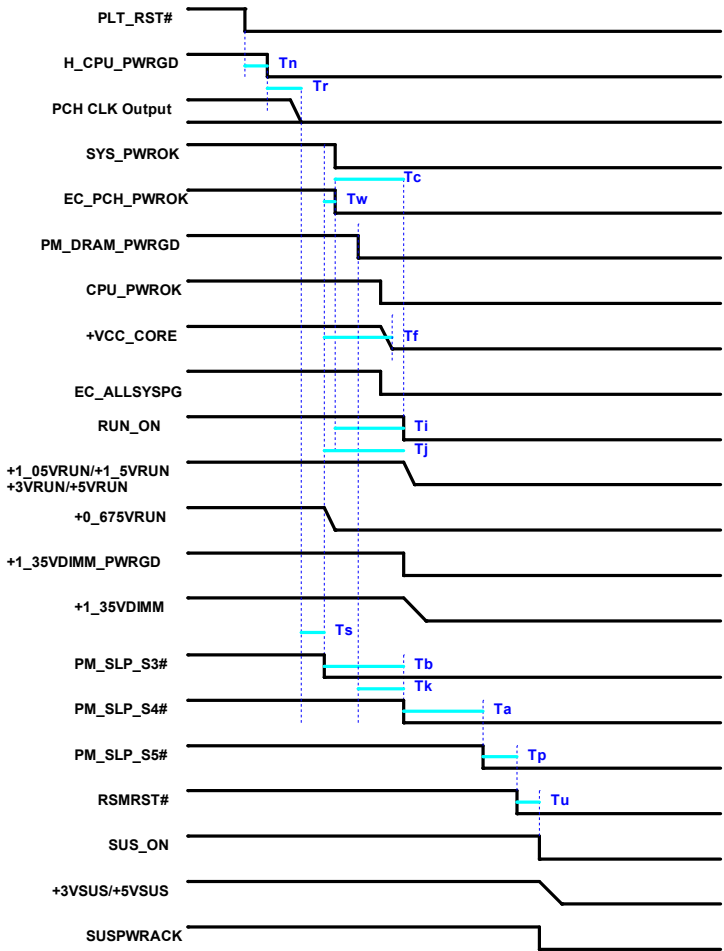
1. The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2. The ramp up overshoot should not exceed the silicon reliability limit voltagr.
3. A VDD33 must ramp up to 90% before NVVDD and PEX VDD in sequence can ramping up.  
NVVDD must ramp up to 90% before FBVDD/Q in sequence can ramping up.
3. No signal should be applied to the GPU before the power rails are fully ramped.
4. Refer to JEDEC Memory Specification for memory related power sequencing.

# MS-16H5 Power on Block Diagram



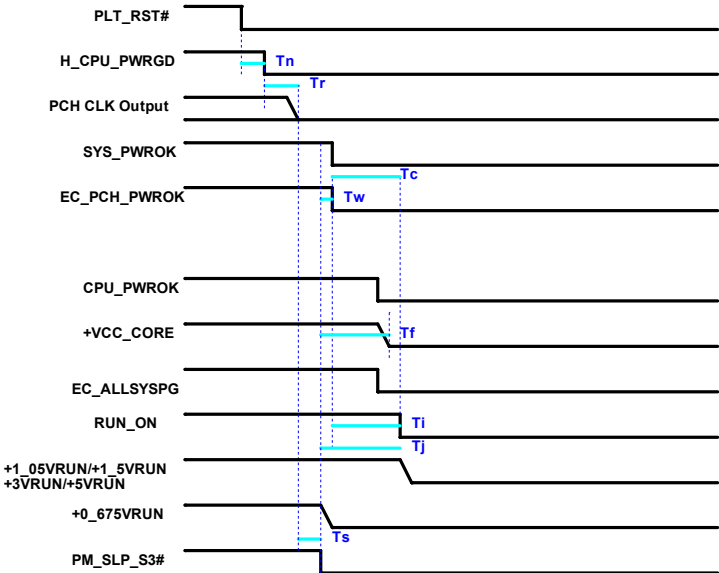
Power down Sequence

S0 -> G3



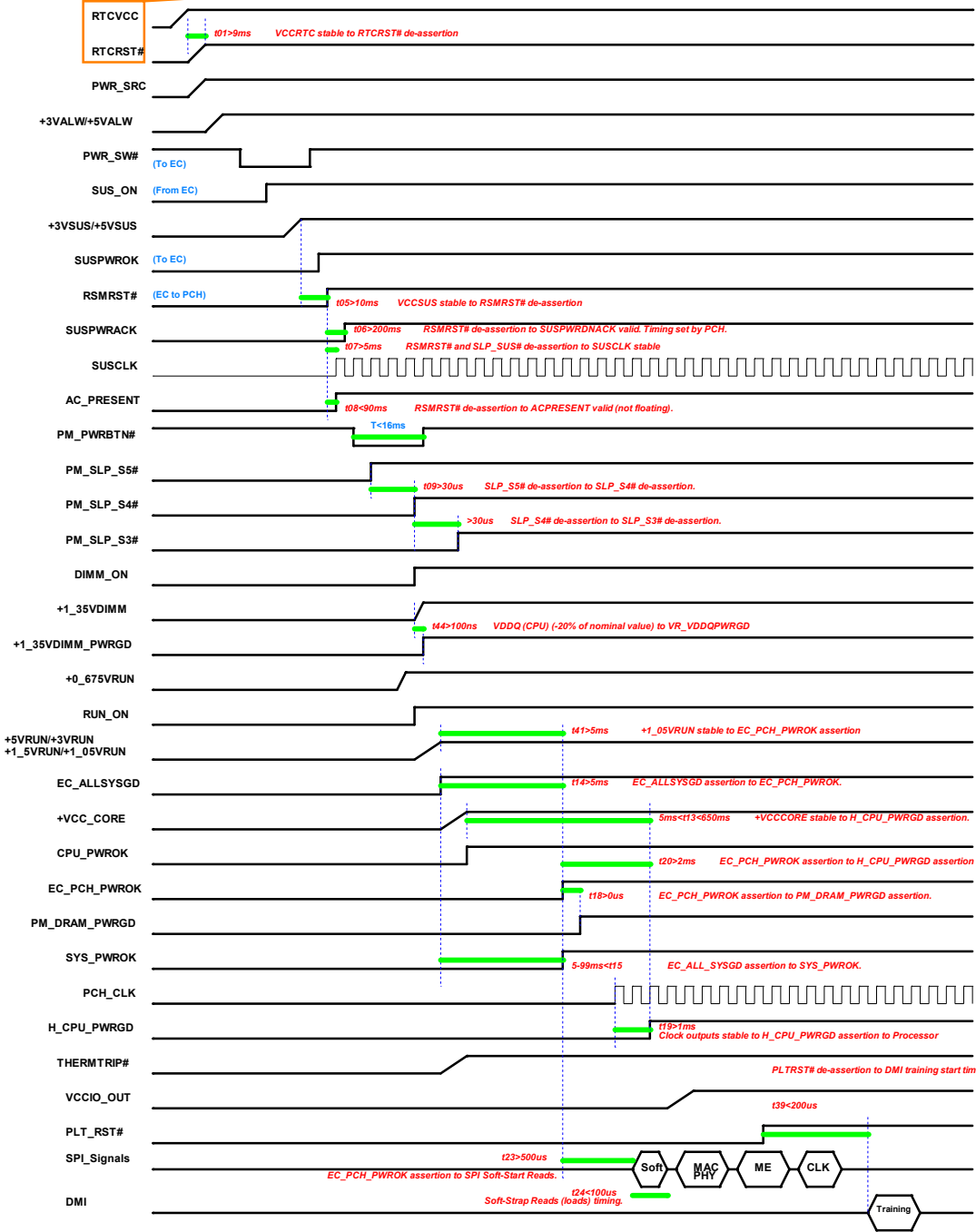
	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3

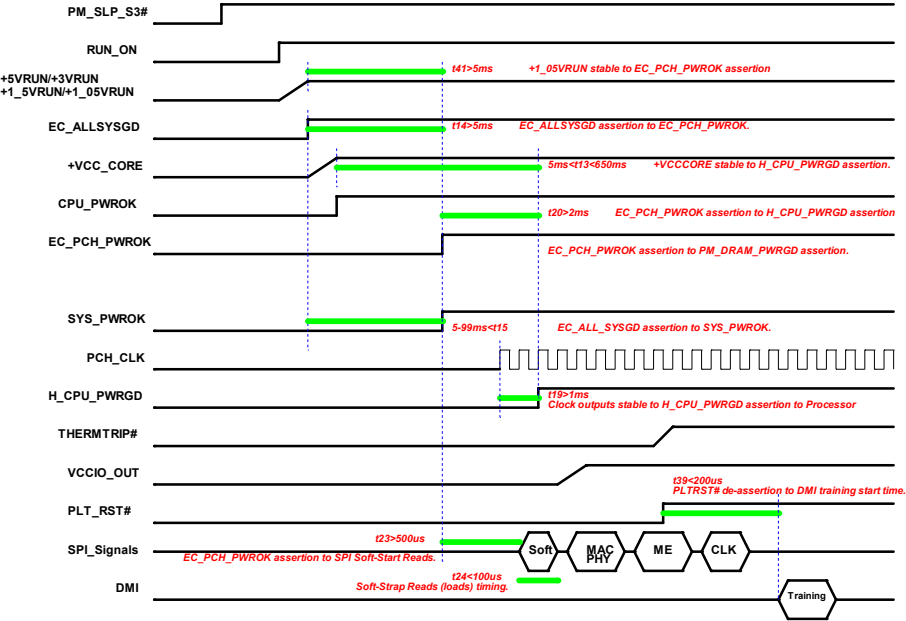


Power on Sequence

G3 -> S0



S3-> S0



# History

## 1.1: 2014/7/3

01. P32 ADD R419 R418 R110  
ADD Q25 Q26  
ADD C709
02. P36 ADD R108 TO DGPU\_PWR\_EN#
03. P43 ADD R408 TO FPC15 PIN4  
ADD R409 TO FPC15 PIN5  
ADD R410 TO FPC15 PIN6  
ADD R411 TO FPC15 PIN7  
ADD R412 TO FPC15 PIN8  
ADD R413 TO FPC15 PIN9  
ADD R414 TO FPC15 PIN10  
ADD R415 TO FPC15 PIN11  
ADD R416 TO FPC15 PIN12

## 2014/7/8

01. P56 Remove JNC6

## 2014/7/10

01. P43 ADD C770 TO +5VSUS\_KB



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History		
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